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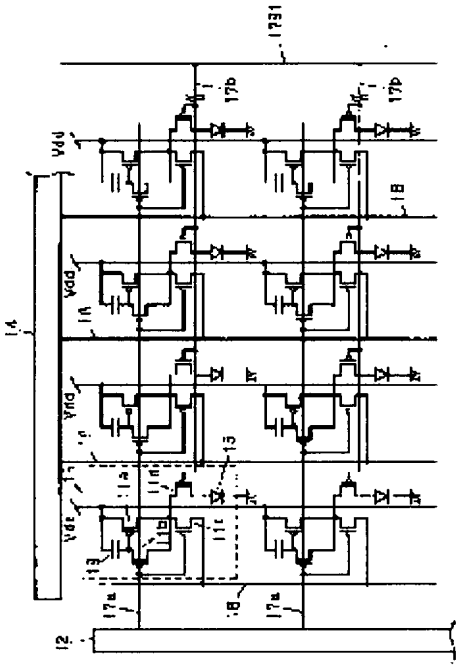
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : TAKAHARA HIROSHI

(54) METHOD FOR DRIVING EL DISPLAY DEVICE AND EL DISPLAY DEVICE AND ITS MANUFACTURING METHOD, AND INFORMATION DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an EL (electroluminescent) display device capable of realizing easily a three-side free constitution.
SOLUTION: In this EL display device, each pixel 16 is constituted of four TFTs (thin film transistor) 11 and the data outputted to a source signal line 18 from a source driver 14 are written in a capacitor 19 so that the luminance of an EL element 15 becomes larger than a prescribed luminance by controlling ON/OFF of the TFTs 11b, 11c with a gate signal line 17a which is connected to a gate driver 12. ON/OFF of the TFT 11d connected to a gate signal line 17b is operated to control a current to the EL element 15. The gate signal line 17b makes the EL element 15 emit light with luminance higher than the prescribed luminance for every block and makes the EL element 15 to be a prescribed luminance by controlling ON/OFF of the element with an ON/OFF signal which is applied by a lighting control line 1791 which is connected for every plural pixel rows.



Drawings are not displayable due to the volume of the data (more than 200 drawings).

CLAIMS

[Claim(s)]
[Claim 1]An EL display which is provided with the following and characterized by forming said controlling signal line so that it may become common to two or more pixel rows.
An EL element which is an active-matrix type EL display and was formed in each pixel.
A driver element which supplies current to said EL element.
Said driver element and a switching element arranged between said EL elements.
A controlling signal line which controls said switching element.

[Claim 2]An EL display which is provided with the following, is formed and is characterized by connecting a pixel row which adjoined to a different controlling signal line so that it may become common [said controlling signal line] to two or more pixel rows.
An EL element which is an active-matrix type EL display and was formed in each pixel.
A driver element which supplies current to said EL element.
Said driver element and a switching element arranged between said EL elements.
A controlling signal line which controls said switching element.

[Claim 3]An EL element formed in each pixel, and a driver element which supplies current to said EL element, Said driver element and the 1st switching element arranged between said EL elements, The 1st controlling signal line that controls said 1st switching element, and the 2nd switching element that impresses voltage to one terminal of said EL element, An EL display, wherein provide the 2nd controlling signal line that controls said 2nd switching element, said 1st controlling signal line and the 2nd controlling signal line are formed so that it may become common to two or more pixel rows, said 1st controlling signal line and the 2nd controlling signal line take a synchronization and a control signal is impressed.
[Claim 4]An EL display which having the following, forming on a substrate a driver circuit which chooses said pixel simultaneously with said pixel, and forming so that a controlling signal line which controls said switching element may become common to two or more pixel rows.
Each pixel is an EL element.
A driver element which supplies current to said EL element.
Said driver element and a switching element arranged between said EL elements.

[Claim 5]An EL display which is provided with the following, is formed so that a controlling signal line which controls said switching element may become common to two or more pixel rows, and is characterized by loading both said source drivers IC and said gate driver IC into one side of a viewing area.
A pixel formed in matrix form.
A source drivers IC which outputs a video signal.
Said pixel is chosen, gate driver IC which impresses a video signal which said source drivers IC outputs is provided, and each pixel is an EL element.
A driver element which supplies current to said EL element, and said driver element and a switching element arranged between said EL elements.

[Claim 6]A drive method of an EL display, wherein it is a drive method of an EL display, display some screens, it changes other portions into a non-display state, it moves a viewing area one by one in a sliding direction of a screen and said moving speeds differ in a portion of a screen.
[Claim 7]A drive method of an EL display changing display luminance by changing the number of times which is a drive method of an EL display and is chosen in the 1st portion of a screen, and the 2nd portion.
[Claim 8]An information display device comprising:
An EL element formed in each pixel.
A driver element which supplies current to said EL element.
Said driver element and a switching element arranged between said EL elements.
An EL display formed so that it might have a controlling signal line which controls said switching element and said controlling signal line might become common to two or more pixel rows, a down converter, an up converter, a receiver, and a speaker.

[Claim 9]An information display device which is provided with the following and characterized by said sealing plate closing both said driver IC and an EL element.
The 1st substrate with which an EL element was formed in matrix form.
A driver IC loaded into said substrate.
A sealing plate which protects said EL element.

[Claim 10]An information display device which is provided with the following and characterized by constituting said display panel so that a position can be changed with a predetermined fulcrum, and comprising the 1st state so that a display image of said display panel can be observed and a mirror of a rear face of said display panel can be observed in the 2nd state.
A display panel in which a pixel was formed in matrix form.
A mirror formed in a rear face of said display panel.
A case in which said display panel was attached.

[Claim 11]An information display device constituting so that an entry content of said ten key may change by having the following and pressing down said function key and a ten key simultaneously.
A display panel in which a pixel was formed in matrix form.
A case in which said display panel was attached.
A photosensor which detects a luminosity of outdoor daylight.
A ten key and a function key arranged at the side or a rear face of said case.

[Claim 12]An EL display which it has the following, a thin film transistor is formed in each lighting part of said pixel, and said white lighting part is formed from material of red, green, and a blue lighting part, and is characterized by arranging said pixel at matrix form.
It is an EL display and 1 pixel is a red lighting part.
A green lighting part.
A blue lighting part.
A white lighting part.

[Claim 13]An EL display characterized by being an opposite direction by a pixel row which it has the following, a thin film transistor is formed in each lighting part of said pixel, and said pixel has been arranged at matrix form, and arrangement of a lighting part of each color of said pixel adjoined.
It is an EL display and 1 pixel is a red lighting part.
A green lighting part.
A blue lighting part.

[Claim 14]An EL display, wherein a gate driver circuit is formed simultaneously with a pixel on a substrate, and EL film is formed in said gate driver time on the street and a metal membrane which was united with an anode electrode is formed on said EL film.
[Claim 15]An EL display in which a gate driver circuit is formed simultaneously with a pixel on a substrate, and EL film is formed in said gate driver time on the street, and a metal membrane which was united with an anode electrode is formed on said EL film, and said metal membrane is characterized by unevenness or being formed circularly corresponding to a pixel.
[Claim 16]The 1st process of forming a pixel circuit which drives a pixel to the 1st substrate, and the 2nd process of forming an insulator layer on said pixel circuit after said 1st process, The 3rd process of forming a mask on said insulator layer and forming said insulator layer circularly via said mask corresponding to a pixel, A manufacturing method of an EL display panel performing the 4th process of forming a picture element electrode on said insulator layer, the 5th process of forming EL film on said picture element electrode, the 6th process of forming a common electrode which consists of metal on said EL film, and the 7th process of forming a protective film on said common electrode.

[Translation done.]

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]the EL display panel in which this invention mainly displays a picture with spontaneous light -- and it is related with information display devices, such as a cellular phone using these EL display panels, etc.
[0002]
[Description of the Prior Art]Since many liquid crystal display panels to a portable equipment etc. are adopted from the advantage of low power consumption with a thin shape, they are used for apparatus, such as a word processor, a personal computer, television, the viewfinder of a video camera, a monitor, etc.
[0003]
[Problem(s) to be Solved by the Invention]However, since liquid crystal display panels are not spontaneous optical devices, there is a problem that it cannot be displayed that a picture does not use a back light. Since predetermined thickness was required in order to constitute a back light, there was a problem that the thickness of a display module became large. In order for a liquid crystal display panel to perform a colored presentation, it is necessary to use a light filter. Therefore, there was a problem that efficiency for light utilization was low.
[0004]
[Means for Solving the Problem]In the 1st EL display in order to solve this technical problem, this invention, An EL element which is an active-matrix type EL display and was formed in each pixel, A driver element which supplies current to said EL element, said driver element and a switching element arranged between said EL elements, and a controlling signal line which controls said switching element are provided, and said controlling signal line is formed so that it may become common to two or more pixel rows.
[0005]An EL element which is an active-matrix type EL display and was formed [2nd] in each pixel in an EL display, A driver element which supplies current to said EL element, and said driver element and a switching element arranged between said EL elements, A controlling signal line which controls said switching element is provided, it is formed and a pixel row which adjoined is connected to a different controlling signal line so that it may become common [said controlling signal line] to two or more pixel rows.
[0006]An EL element formed [3rd] in each pixel in an EL display, and a driver element which supplies current to said EL element, Said driver element and the 1st switching element arranged between said EL elements, The 1st controlling signal line that controls said 1st switching element, and the 2nd switching element that impresses voltage to one terminal of said EL element, The 2nd controlling signal line that controls said 2nd switching element is provided, said 1st controlling signal line and the 2nd controlling signal line are formed so that it may become common to two or more pixel rows, said 1st controlling signal line and the 2nd controlling signal line take a synchronization, and a control signal is impressed.
[0007]A driver element by which each pixel supplies [4th] current to an EL element and said EL element in an EL display, It has said driver element and a switching element arranged between said EL elements, and a driver circuit which chooses said pixel is formed on a substrate simultaneously with said pixel, and it is formed so that a controlling signal line which controls said switching element may become common to two or more pixel rows.
[0008]A pixel formed [5th] in matrix form in an EL display, Provide a source drivers IC which outputs a video signal, and gate driver IC which impresses a video signal which chooses said pixel and said source

drivers IC outputs, and each pixel An EL element, It has a driver element which supplies current to said EL element, and said driver element and a switching element arranged between said EL elements, It is formed so that a controlling signal line which controls said switching element may become common to two or more pixel rows, and both said source drivers IC and said gate driver IC are loaded into one side of a viewing area.

[0009]In a drive method of an EL display, some screens are displayed, other portions are changed into a non-display state, a viewing area is moved to a sliding direction of a screen one by one, and said moving speeds differ [6th] in a portion of a screen.

[0010]Display luminance is changed by changing the number of times chosen [7th] in the 1st portion of a screen, and the 2nd portion in a drive method of an EL display.

[0011]An EL element formed [8th] in each pixel in an information display device, and a driver element which supplies current to said EL element, An EL display formed so that it might have said driver element, a switching element arranged between said EL elements, and a controlling signal line which controls said switching element and said controlling signal line might become common to two or more pixel rows, A down converter, an up converter, a receiver, and a speaker are provided.

[0012]Providing the 1st substrate with which an EL element was formed [9th] in matrix form in an information display device, a driver IC loaded into said substrate, and a sealing plate which protects said EL element, said sealing plate is closing both said driver IC and an EL element.

[0013]A display panel in which a pixel was formed [10th] in matrix form in an information display device, A mirror formed in a rear face of said display panel and a case in which said display panel was attached are provided, Said display panel is constituted so that a position can be changed with a predetermined fulcrum, and it comprises the 1st state so that a display image of said display panel can be observed and a mirror of a rear face of said display panel can be observed in the 2nd state.

[0014]A display panel in which a pixel was formed [11th] in matrix form in an information display device, A case in which said display panel was attached, and a photosensor which detects a luminosity of outdoor daylight, By providing a ten key and a function key arranged at the side or a rear face of said case, and pressing down said function key and a ten key simultaneously, it is constituted so that an entry content of said ten key may change.

[0015]A lighting part in an EL display in which 1 pixel is [12th] as green as a red lighting part, A blue lighting part and a white lighting part are provided, a thin film transistor is formed in each lighting part of said pixel, said white lighting part is formed from material of red, green, and a blue lighting part, and said pixel is arranged at matrix form.

[0016]A lighting part in an EL display in which 1 pixel is [13th] as green as a red lighting part, It is an opposite direction by a pixel row which a blue lighting part is provided, a thin film transistor is formed in each lighting part of said pixel, and said pixel has been arranged at matrix form, and arrangement of a lighting part of each color of said pixel adjoined.

[0017]In an EL display, a gate driver circuit is formed simultaneously with a pixel on a substrate, and EL film is formed in said gate driver time on the street, and a metal membrane which was united with an anode electrode is formed [14th] on said EL film.

[0018]In an EL display, a gate driver circuit is formed [15th] simultaneously with a pixel on a substrate, EL film is formed in said gate driver time on the street, and a metal membrane which was united with an anode electrode is formed on said EL film, and said metal membrane is characterized by unevenness or being formed circularly corresponding to a pixel.

[0019]The 1st process of forming a pixel circuit which drives [16th] a pixel to the 1st substrate in a manufacturing method of an EL display panel, The 2nd process of forming an insulator layer on said pixel circuit after said 1st process, The 3rd process of forming a mask on said insulator layer and forming said insulator layer circularly via said mask corresponding to a pixel, The 4th process of forming a picture element electrode on said insulator layer, the 5th process of forming EL film on said picture element electrode, the 6th process of forming a common electrode which consists of metal on said EL film, and the 7th process of forming a protective film on said common electrode are performed.

[0020]

[Embodiment of the Invention]In this specification, each drawing has an abbreviation and the part which carried out scaling in order to draw an understanding easily. For example, with the sectional view of the display panel of drawing 5, the sealing film 73 etc. are illustrated thickly enough. In drawing 6, the thin film transistor (TFT) etc. which impress a signal to a picture element electrode are omitted. Adding timely is desirable although the phase film for phase compensation, etc. are omitted in the display panel of this invention. The above thing is the same also to other drawings. The part which attached the same number

or the sign has the same material, a function, or operation.
[0021]Especially the contents explained with each drawing are combinable with other examples, even if there is no notice. For example, a touch panel etc. can be added to the display panel of drawing 6, and it can be considered as an information display device as shown in Drawing 199 and Drawing 210. A magnifying lens can be attached and viewfinders (refer to Drawing 206), such as a video camera (refer to Drawing 130), can also be constituted. The drive method of this invention explained with drawing 38, drawing 39, drawing 49, Drawing 216, etc. is applicable to either the display of this invention, or a display panel. It cannot be overemphasized that it is not limited to this although this invention mainly explains the active-matrix type display panel in which TFT was formed in each pixel, and it can apply also to a simple matrix type.
[0022]Thus, it can combine mutually and especially the matter, contents, and specification that were explained with the specification and the drawing can be made to apply, even if not illustrated.
[0023](Embodiment 1) The organic electroluminescence display panel which is low power consumption, is high indication quality, and also is constituted by arranging two or more organic electroluminescence (EL) elements to matrix form as a display panel which can be slimmed down attracts attention now.
[0024]As an organic electroluminescence display panel is shown in drawing 2, the organic electroluminescence layer 47 of at least one layer which consists of an electron transport layer, a luminous layer, an electron hole transporting bed, etc. on the array substrate 49 in which the transparent electrode as the picture element electrode 48 was formed, and the reflection film 46 are laminated. The organic electroluminescence layer 47 emits light by applying the voltage of plus and the minus to the negative pole (cathode) of the reflection film 46 to the anode (anode) of the transparent electrode (picture element electrode) 48, and impressing a direct current among these. Thus, an EL display panel can be equal to practical use by using the organic compound which can expect a good luminescent characteristic for an organic electroluminescence layer.
[0025]A cathode terminal, an anode electrode, or a reflection film may form and constitute the optical interference film which becomes an ITO electrode from a dielectric multilayer. A dielectric multilayer is what carried out multilayer formation of the dielectric film of a low refractive index, and the dielectric film of a high refractive index by turns (dielectric mirror). This dielectric multilayer has a function (screen effect) which makes good the color tone of the light emitted from organic electroluminescence structure.
[0026]Big current flows into the wiring 63 and 51 which supplies current to an anode or a cathode. For example, if the screen size of an EL display turns into 40 inch sizes, about [100A] current will flow. Therefore, it is necessary to produce the resistance of these wiring low enough. By this invention, wiring of an anode etc. is first formed with a thin film to this technical problem. And the thickness of a conductor is thickly formed in this thin film wiring by electrolysis plating art. The wiring itself or the metallic wiring which turns into wiring from **** is added if needed.
[0027]In order to supply big current to an anode or cathode wiring, it wires from a current supply source means to the neighborhood, such as said anode wiring, using the power wiring of a small current by high tension, and the low voltage and high electric current are converted the power and supplied using a DCDC converter etc. That is, it wires from a power supply to a power consumption object using high tension and small current wiring, and changes into a high current and the low voltage the neighborhood [for power consumption]. A DCDC converter, a transformer, etc. are illustrated as such a thing.
[0028]It is preferred to use for the reflection film 46 the thing which has small work functions, such as lithium, silver, aluminum, magnesium, indium, copper, or each alloy, especially an aluminum-Li alloy. A big conductive material or gold of a work function, such as ITO (tin dope indium oxide), etc. can be used for the transparent electrode (picture element electrode) 48. When gold is used as an electrode material, an electrode will be in a translucent state. Other materials, such as IZO, may be sufficient as ITO. This matter is the same also to a picture element electrode.
[0029]When vapor-depositing a thin film to the picture element electrode 48 etc., it is good to form an organic electroluminescence film in argon atmosphere. By forming a carbon film at not less than 20 nm 50 nm or less on ITO as the picture element electrode 48, the stability of an interface improves and light emitting luminance and luminous efficiency will also become good.
[0030]It cannot be overemphasized that it is not limited to forming an organic electroluminescence film by vacuum evaporation, and may form by an ink jet.
[0031](Embodiment 2) Hereafter, in order to make easy an understanding of the EL display panel structure of this invention, the manufacturing method of the organic electroluminescence display panel of this invention is explained first.
[0032]In order to improve heat dissipation nature, the array substrate 49 may be formed with sapphire

glass. Or a thermally conductive good thin film or thick film may be formed. For example, using the substrate in which diamond membrane was formed is illustrated. Of course, a quartz glass substrate and a soda glass substrate may be used. In addition, the metal plate which consists of ceramic substrates, copper, etc., such as alumina, may be used, or what coated the insulator layer with the metal membrane for vacuum evaporation or spreading may be used. Since light is emitted from the direction of the surface of a substrate as a substrate material when using a picture element electrode as a reflection type, impermeable material, such as stainless steel besides the transparence of glass, quartz, resin, etc. thru/or a translucent material, can also be used. This composition is illustrated to drawing 5. In drawing 5, the cathode terminal is formed with the transparent electrodes 72, such as ITO.

[0033]Although it presupposed that a cathode etc. are formed with a metal membrane in the example of this invention, it is not limited to this and may form by transparent membranes, such as ITO and IZO. Thus, a transparent EL display panel can be constituted by using the electrode of both the anode of EL element 15, and a cathode as a transparent electrode. That is, it can have composition whose other side of a display panel is almost transparent and which is in sight by raising transmissivity to about 80%, without using a metal membrane, displaying a character and a picture.

[0034]A plastic plate may be used for the array substrate 49. It can be hard to break a plastic plate, and since it is lightweight, it is the optimal as a substrate for display panels of a cellular phone. As for a plastic plate, it is preferred to paste an auxiliary substrate together to one field of the base board used as a core material with adhesives, and to use as a laminated circuit board. Of course, these substrates may not be limited to a board and a with a 0.05 mm or more 0.3 mm or less thickness film may be sufficient as them.

[0035]As a material of a base board, it is preferred to use alicyclic polyolefin resin. ARTON by Japan Synthetic Rubber Co., Ltd. (200-micrometer-thick single board) is illustrated as such alicyclic polyolefin resin. The hard court layer which has heat resistance, solvent resistance, or a moisture permeability-proof function in one field of a base board, And the auxiliary substrate (or a film or a film) which consists of polyester resin, polyethylene resin, or polyether sulfone resin etc. in which the gas barrier layer with an infiltrative-proof function was formed is arranged.

[0036]Thus, since the array substrate 49 comprises a base board and an auxiliary substrate of two sheets when it constitutes the array substrate 49 from a plastic, The auxiliary substrate (or a film or a film) which consists of polyether sulfone resin etc. in which the hard court layer and the gas barrier layer were formed in the field of another side of a base board as well as the above-mentioned is arranged. A base board and an auxiliary substrate are pasted together via adhesives or a binder, and let them be a laminated circuit board.

[0037]As for using as adhesives what consists of acrylic resin with UV (ultraviolet rays) hardening type, and an acrylic resin, it is preferred to use what has a fluorine group. In addition, the adhesives or the binder of an epoxy system may be used. As for the refractive index of adhesives or a binder, it is preferred to use or more 1.47 1.54 or less thing. It is preferred to make it refractive index difference with the refractive index of the array substrate 49 become 0.03 or less. As for especially adhesives, it is preferred to add optical dispersing agents, such as titanium oxide which was indicated previously, and to make it function as a light scattering layer.

[0038]When pasting each auxiliary substrate together to a base board, it is good to make still more preferably into 100 degrees or less (about 90 degrees) the angle which the optical lagging axes of each auxiliary substrate make 80 degrees or more 120 degrees or less 45 degrees or more. By using this range, the phase contrast generated with polyether sulfone resin etc. which are an auxiliary substrate and an auxiliary substrate can be thoroughly negated within a laminated circuit board. Therefore, the plastic plate for organic electroluminescence display panels can be treated now as an isotropic substrate without phase contrast.

[0039]By this composition, flexibility spreads remarkably compared with a film substrate or a film laminated circuit board with phase contrast. That is, it is because linear polarization can be changed into elliptical polarization by combining a phase difference film as a design. If there is phase contrast in the array substrate 49 etc., an error with a designed value will occur according to this phase contrast.

[0040]Epoxy system resin, urethane system resin, or acrylic resin can be used for the hard court layer in an auxiliary substrate as a material, and it serves as the 1st undercoat layer of a transparent conducting film that has a stripe like electrode or a picture element electrode. As a gas barrier layer, organic materials, such as inorganic materials, such as SiO_2 and SiOx, or poly vinyl alcohol, and polyimide, etc. can be used.

As a binder, adhesives, etc., epoxy adhesive, polyester system adhesives, etc. other than acrylic which were described previously can be used. Although the thickness of a glue line shall be 100 micrometers or less, in order to smooth unevenness of the surfaces, such as a substrate, it is preferred to be referred to

as not less than 10 micrometers.
[0041]It is preferred to use a with a not less than 40-micrometer thickness [400 micrometer or less] thing as the auxiliary substrate and auxiliary substrate which constitute the array substrate 49. Since the unevenness or phase contrast at the time of melting extrusion molding called the die line of polyether sulfone resin by the thickness of each auxiliary substrate being 120 micrometers or less can be suppressed low, thickness shall be not less than 50 micrometers 80 micrometers or less preferably.
[0042]Next, SiOx is formed in this laminated circuit board as an auxiliary undercoat layer of a transparent conducting film, and the transparent conducting film which consists of ITO used as a picture element electrode is formed with weld slag art. Thus, the transparent conducting film of the manufactured plastic plate for organic electroluminescence display panels can realize sheet-resistance-values 25ohm/**, and 80% of transmissivity as the membrane characteristics.
[0043]When thin, in the manufacturing process of an organic electroluminescence display panel, the plastic plate for organic electroluminescence display panels will curl by heat treatment, so that the thickness of a base board may be 50 micrometers - 100 micrometers. A crack occurs in ITO which constitutes a stripe like electrode etc., and conveyance after it becomes impossible. A good result is not obtained in connection of a circuit component. However, when a base board is not less than 200-micrometer500 micrometers or less in thickness with a single board, there is no modification of a substrate and it excels in smooth nature, and conveyance nature is good and, as for the transparent conducting film characteristic, is stabilized. Connection of a circuit component can also be made satisfactorily. Since it has moderate pliability and smoothness, it is considered to be good that thickness shall be not less than 250 micrometers 450 micrometers or less.
[0044]When using organic materials, such as the above-mentioned plastic plate, as the array substrate 49, it is preferred to form the thin film which consists of inorganic materials as a barrier layer also in the field which touches a liquid crystal layer. As for the barrier layer which consists of this inorganic material, being formed with an AIR coat and an identical material is preferred. The closure lid 41 is also producible by the same art or composition as the array substrate 49.
[0045]When forming a barrier layer on a picture element electrode or a stripe like electrode, in order to reduce the loss of the voltage impressed to a light modulation layer as much as possible, it is preferred to use a low dielectric constant material. For example, the amorphous carbon film (specific inductive capacity 2.0-2.5) which added fluoride is illustrated. In addition, the LKD series (LKD-T200 series (specific inductive capacity 2.5-2.7)) and LKD-T400 series (specific inductive capacity 2.0-2.2) which JSR is manufacturing and selling are illustrated. LKD series is the spin spreading type which used MSQ (methy-silsesquioxane) as the base, and its specific inductive capacity is also low [as 2.0-2.7] preferred. In addition, inorganic materials, such as organic materials, such as polyimide, urethane, and an acrylic, SiNx, SiO_2, may be sufficient. It is satisfactory even if it uses such barrier layer materials for an auxiliary substrate.
[0046]There is also an advantage that the advantage that it cannot divide by using the array substrate 49 or the closure lid 41 formed with the plastic and that a weight saving can be carried out can be demonstrated, and also press working of sheet metal can be carried out. That is, I hear that the substrate of arbitrary shape can be produced by press working of sheet metal or cutting, and it is (see drawing 3). Arbitrary shape and thickness are also processible by fusion or chemicals processing. For example, making it circular, making it globular forms (curved surface etc.), or processing conical shape is illustrated. By press working of sheet metal, the uneven part 252 can be formed in one substrates face, and, simultaneously with manufacture of a substrate, formation of the diffusing surface or embossing can be performed.
[0047]It is also easy to form in the hole of the array substrate 49 formed by carrying out press working of sheet metal of the plastic so that a back light or the gage pin of a cover substrate can be inserted. Electric circuits formed by thick film technique or a thin film technology in the array substrate 49 and the closure lid 41, such as a capacitor or resistance, may be constituted. By forming a crevice (not shown) in the closure lid 41, forming the heights 251 in the array substrate 49, and forming so that these crevice and heights can be inserted in exactly, it may constitute so that the closure lid 41 and the array substrate 49 can be unified by insertion.
[0048]When a glass substrate was used, the bank used when vapor-depositing an EL element to the periphery of the pixel 16 was formed. 1.0 micrometers or more 3.5 micrometers or less of banks (rib) are formed in the shape of heights still more preferably using a resin material by not less than 1.5-micrometer a thickness of 2.5 micrometers or less. The bank (heights) 251 which consists of this resin is also simultaneously [with formation by press working of sheet metal of the closure lid 41 or the array substrate 49] producible (see drawing 3). This is a big effect generated by forming the closure lid 41 and the array

substrate 49 by resin. SOG material besides an acrylic resin and polyimide resin may be sufficient as bank material.

[0049]Thus, since production time can be shortened by forming a resin part simultaneously with a substrate, low-cost-izing is possible. The heights 251 are formed in dot form at a display area part at the time of manufacture of the array substrate 49 etc. These heights 251 are forming between adjacent pixels, and hold the predetermined space of the closure lid 41 and the array substrate 49. Stripe shape besides the shape of ** which encloses a picture element electrode may be sufficient as bank shape.

[0050]Although it presupposed that the heights 251 which function as a bank are formed in the above example, it is not limited to this. For example, it is good also as investigating a picture element part by press working of sheet metal etc. (crevice). The method which the uneven part 252 and the heights 251 are formed simultaneously with a substrate, and also form a flat surface substrate first, press by reheating after that, and forms unevenness is also contained.

[0051]The light filter of mosaic shape may be formed by coloring the closure lid 41 and the array substrate 49 directly. Art, such as ink jet printing, is used for a substrate, and a color, coloring matter, etc. are applied and are made to permeate. It is made to dry at an elevated temperature after osmosis, and what is necessary is just to cover the surface with inorganic materials, such as resin, such as UV resin, silicon oxide, or nitrogen oxide. A light filter may be formed with gravure printing technique, offset-printing art, the semiconductor pattern formation art of applying and developing a film with a spinner, etc. the black matrix (BM) in black, a dark color, or the complementary color relation of light to modulate may be directly formed by coloring using the same art besides a light filter. A crevice may be formed so that it may correspond to a pixel on a substrates face, and it may constitute so that a light filter, BM, or TFT may be embedded in this crevice. It is preferred to carry out the tunic of the surface with an acrylic resin especially. With this composition, there is also an advantage that a picture element electrode side etc. are smoothed.

[0052]Resin of a substrate face may be electric-conduction-ized by a conductive polymer etc., and a picture element electrode or a cathode terminal may be constituted directly. A hole is greatly made in a substrate and the composition which inserts electronic parts, such as a capacitor, in this hole is also illustrated. Thereby, the advantage which a substrate can constitute thinly is demonstrated.

[0053]A pattern may be freely formed by cutting the surface of a substrate. It may form by melting the periphery of the closure lid 41 and the array substrate 49. In the case of an organic electroluminescence display panel, the periphery of a substrate may be melted and closed in order to prevent penetration of the moisture from the outside.

[0054]As mentioned above, the drilling process to a substrate is easy by forming a substrate by resin. Press working of sheet metal etc. can constitute substrate shape freely.

[0055]Since the closure lid 41 and the array substrate 49 can be used as a multilayered circuit board or a double-sided board, it is possible to make a hole in the closure lid 41 and the array substrate 49, to fill up this hole with electric conduction resin etc., and to also make it flow through the table and the reverse side of a substrate electrically.

[0056]It is good also considering the closure lid 41 and array substrate 49 self as a multilayer wiring board. For example, the terminal of electronic parts, such as a capacitor, is fitted over the hole which inserted the current-carrying pin etc. instead of electric conduction resin, or was formed, or the circuit wiring by a thin film, a capacitor, a coil, or resistance may be formed in a substrate. Since multilayering is constituted by pasting a thin substrate together, one or more of the substrates (film) to paste together may be colored in this case.

[0057]A color and coloring matter are added to a substrate material, it can be colored the substrate itself or a filter can be formed. A serial number can also be formed simultaneously with substrate production. Malfunction can be prevented by light being irradiated by the loaded IC chip by coloring only portions other than a viewing area.

[0058]The half of the viewing area of a substrate can also be colored a different color. This should just apply resin board processing technology (injection processing, complexion processing, etc.). The half of a viewing area can also be made into different EL layer thickness by using the same processing technology. An indicator and a circuit part can also be formed simultaneously. It is also easy to change the substrate thickness of a viewing area and a driver loading field.

[0059]A micro lens can also be formed in the closure lid 41 or the array substrate 49 so that it may correspond to a pixel, or so that it may correspond to a viewing area. A diffraction grating may be formed by processing the closure lid 41 and the array substrate 49. By forming unevenness more detailed enough than pixel size, an angle of visibility can be improved or view angle dependence can be given. Processing of such arbitrary shape, ultra-fine processing technology, etc. are realizable with the La Stampa art which

forms the micro lens which OMRON Corp. developed.
[0060]The stripe like electrode (not shown) is formed in the closure lid 41 and the array substrate 49. When an antireflection film (AIR coat) is formed in the field where a substrate touches air and other components, such as a polarizing plate (polarization film), are stuck on it, an antireflection film (AIR coat) is formed in the surface of the component, etc. When the polarizing plate etc. are not stuck on the closure lid 41 and the array substrate 49, an antireflection film (AIR coat) is directly formed in the closure lid 41 and the array substrate 49.
[0061]Although the above example has been described focusing on the closure lid 41 and the array substrate 49 being formed with a plastic, it is not limited to this. For example, even if the closure lid 41 and the array substrate 49 are a glass substrate and a metal substrate, press working of sheet metal, cutting, etc. can form or constitute the uneven part 252, the heights 251, etc. It is not limited to a substrate, either. For example, a film or a sheet may be sufficient.
[0062]In order to prevent or control adhesion of the garbage to the surface of a polarizing plate, it is effective to form the thin film which consists of fluoro-resins. Conductor films which have a hydrophilic group for a static free, such as a thin film, a conductive polymer film, and a metal membrane, may be applied or vapor-deposited.
[0063]The polarizing plate (polarization film) arranged or formed in the light incidence face or light emitting surface of the display panel 82 is not limited to what carries out linear polarization, and may serve as elliptical polarization. Two or more polarizing plates may be pasted together, a polarizing plate and a phase difference plate may be combined, or what was pasted together may be used.
[0064]As a main material which constitutes a polarization film, a TAC film (triacetyl cellulose film) is the optimal. A TAC film is because it has the outstanding optical property, surface smoothness, and processing suitability. About manufacture of a TAC film, it is optimal to produce with solution flow casting film production art.
[0065]The composition in which an AIR coat is formed with dielectric monolayer or a multilayer film is illustrated. In addition, resin of the low refractive index of 1.35-1.45 may be applied. For example, the acrylic resin of a fluorine system, etc. are illustrated and or more 1.37 1.42 or less thing has especially a good refractive index.
[0066]An AIR coat has 3 lamination or two-layer composition. In the case of three layers, it is used in order to prevent reflection in the wavelength band region of large visible light, and it calls this a multi-coat. In a two-layer case, it is used in order to prevent reflection in the wavelength band region of specific visible light, and it calls this V coat. A multi-coat and V coat are properly used according to the use of a display panel. An AIR coat may not be limited more than two-layer, and the number of them may be one. In this case, magnesium fluoride (MgF_2) is laminated nd1=lambda/2, and is formed.

[0067]In the case of a multi-coat, optical thickness nd=lambda/4 are laminated for an aluminum oxide (aluminum$_2O_3$), it laminates nd1=lambda/2, and magnesium fluoride (MgF_2) for a zirconium (ZrO_2) nd1=lambda/4, and it forms. Usually, a thin film is formed as a value of lambda= 520 nm or the neighborhood of those.
[0068]In the case of V coat, nd1=lambda/4 or yttrium oxide (Y_2O_3), and magnesium fluoride (MgF_2) are laminated nd1=lambda/4, and silicon monoxide (SiO) is formed for optical thickness nd1=lambda/4, and magnesium fluoride (MgF_2). It is better to use Y_2O_3 also from the stability of a substance, when modulating blue glow since SiO has an absorption band region in the blue side. A SiO_2 thin film may be used. Of course, it is good also as an AIR coat using resin of a low refractive index, etc. For example, acrylic resins, such as fluoride, are illustrated. As for these, it is preferred to use an ultraviolet curing type.
[0069]In order to prevent static electricity from being charged by the display panel, it is preferred that hydrophilic nature constitutes substrate materials, such as to apply resin of hydrophilic nature to the surfaces, such as light guide plates, such as a cover substrate, and the display panel 82, or a panel, from a good material. In addition, in order to prevent surface reflection, embossing may be performed on the surface of the polarizing plate 54, etc.
[0070]The thin film transistor (TFT) as two or more switching elements or current control elements is formed in 1 pixel. Although TFT to form may be the same kind of TFT and it may be TFT of the kind which is different like TFT of P channel type and N channel type, the thin film transistor for switching and the thin film transistor for a drive of the thing of like-pole nature are desirably desirable. The structure of TFT is not limited like planer type TFT, and may also depend that in which a stagger type or a reverse stagger type may be used, and the impurity range (sauce, drain) was formed using the self aryne method on a non-

self aryne method.
[0071]EL element 15 of this invention has EL structure by which ITO which serves as a hole injection electrode (picture element electrode) on an array substrate, one or more sorts of organic layers, and an electron injection electrode were laminated one by one, and TFT is provided in said array substrate.
[0072]In order to manufacture the EL element of this invention, the array of TFT is first formed on a substrate at desired shape. And ITO which is a transparent electrode (picture element electrode) on a smoothing film is formed and patterned by a sputtering technique. Then, an organic electroluminescence layer, an electron injection electrode, etc. are laminated.
[0073]What is necessary is just to use the usual polycrystalline silicon TFT as TFT. TFT is provided in the end of each pixel of EL structure, and the sizes of the pixel in this case of that size are 20 micrometers x 20 micrometers - 300 micrometers x about 300 micrometers in about 10-30 micrometers.
[0074]The wiring electrode of TFT is provided on an array substrate. The resistance of a wiring electrode is low, and there is a function to electrically connect a hole injection electrode moreover and to hold down resistance low, and, generally the wiring electrode, Although the thing containing any one sort of aluminum, aluminum and a transition metal (however, except for Ti), Ti, or the titanium nitride (TiN) or two sorts or more is used, in this invention, it is not restricted to this material. What is necessary is for the thickness of the whole which combined the hole injection electrode used as the ground of EL structure and the wiring electrode of TFT just to be usually about 100-1000 nm, although there is no restriction in particular.
[0075]An insulating layer is provided between the wiring electrode of TFT11, and the organic layer of EL structure. That in which the insulating layer formed inorganic system materials, such as silicon oxide, such as SiO_2, and silicon nitride, with weld slag or vacuum deposition, As long as the coat etc. of resin system materials, such as a silicon oxide layer formed by SOG (spin one glass), photoresist, polyimide, and an acrylic resin, have insulation, they may be any, but polyimide's are especially preferred. An insulating layer also plays the role of the anticorrosion and the waterproof film which protects a wiring electrode from moisture or corrosion.
[0076]The light emission peak of EL structure may be two or more. For example, the green and the blue light part in the EL element of this invention are obtained with the combination of EL structure of blue-green luminescence, and a green transmission layer or a blue transmission layer. A red light part can be obtained by the fluorescence conversion layer which changes bluish green luminescence of EL structure of blue-green luminescence, and this EL structure into the wavelength near red.
[0077]Next, EL structure which constitutes EL element 15 of this invention is explained. EL structure of this invention is provided with the following.
The electron injection electrode which is a transparent electrode.
One or more sorts of organic layers.
Hole injection electrode.
An organic layer has a hole transporting bed of at least one layer, and a luminous layer, respectively, for example, has an electron injection transporting bed, a luminous layer, an electron hole transporting bed, and a hole injection layer one by one. There may not be any hole transporting bed. The organic layer of EL structure of this invention can be considered as various composition, it may omit electron injection and a transporting bed, may make it a luminous layer and one, or may mix a hole-injection transporting bed and a luminous layer.
[0078]Since it is the structure which takes out the light which emitted light from the hole injection electrode side as a material of a hole injection electrode, ITO (tin dope indium oxide), IZO (zinc dope indium oxide), ZnO, SnO_2, and In_2O_3 etc. are mentioned, but. Especially ITOIZO is preferred. As for the thickness of a hole injection electrode, it is preferred for what is necessary to be just to have the thickness more than [which can perform hole pouring enough] fixed, and to usually be referred to as about 10-500 nm. In order to raise the reliability of an element into the material of a hole injection electrode, it is required for it for driver voltage to be low, but ITO of 10-30ohms / ** (50-300 nm of thickness) is mentioned as a desirable thing. When actually using it, the cross protection by reflection by hole injection electrode interfaces, such as ITO, should just set up the thickness and the optical constant of an electrode fully fill optical extraction efficiency and color purity. Although this hole injection electrode can be formed with vacuum deposition etc., being formed of a sputtering technique is preferred. Sputtering gas in particular is not restricted and inactive gas, such as Ar, helium, Ne, Kr, and Xe, or these mixed gas should just be used for it.
[0079]An electron injection electrode comprises material using the small metal, compound, or alloy of the work function [sputtering technique] preferably formed with vacuum deposition. For example, in order to

raise metallic element simple substances, such as K, Li, Na, Mg, La, Ce, Ca, Sr, Ba, aluminum, Ag, In, Sn, Zn, and Zr, or stability, it is preferred to use the alloy system of two ingredients containing them or three ingredients. As an alloy system, Ag-Mg (Ag:1 - 20at%), aluminum-Li (Li:0.3 - 14at%), In-Mg (Mg:50 - 80at%), aluminum-Ca (Ca:5 - 20at%), etc. are preferred, for example. The thickness of an electron injection electrode thin film should just make electron injection the thickness more than [which can be performed enough] fixed, and should just set it to 1 nm or more preferably 0.1 nm or more. Although there is no restriction in particular in the upper limit, the thickness is just usually about 100-500 nm.

[0080]A hole injection layer has a function which makes easy pouring of the electron hole from a hole injection electrode, and an electron hole transporting bed has a function which bars the function and electron which convey an electron hole, and is also called an electric charge pouring layer and a charge transport layer.

[0081]An electron injection transporting bed is provided when the electron injection transportation function of the compound used for a luminous layer is not so high, and it has a function which bars the function which makes easy pouring of the electron from an electron injection electrode, the function to convey an electron, and an electron hole.

[0082]These hole injection layers, an electron hole transporting bed, and an electron injection transporting bed increase and close the electron hole and electron which are poured in to a luminous layer, a recombination area is made to optimize, and there is work which improves luminous efficiency. An electron injection transporting bed may be separately provided in a layer with a pouring function, and a layer with a transportation function.

[0083]Although the thickness of a luminous layer, the thickness which combined the hole injection layer and the electron hole transporting bed, and the thickness in particular of an electron injection transporting bed are not limited but it changes also with formation methods, it is preferred to usually be referred to as about 5-100 nm.

[0084]What is necessary is just to make them into comparable as the thickness of a luminous layer or 1 / about 10 to 10 times, although the thickness of a hole injection layer and an electron hole transporting bed and the thickness of an electron injection transporting bed are based on the design of a recombination-radiation field. As for the thickness of a hole injection layer and an electron hole transporting bed, and each thickness in the case of dividing an electronic injection layer and an electron transport layer, it is [a pouring layer / 1 nm or more and a transporting bed] preferred to be referred to as not less than 20 nm. The maximum of the thickness of the pouring layer at this time and a transporting bed is [in a pouring layer] usually about 100 nm at about 100 nm and a transporting bed. It is also the same as when providing two layers of pouring transporting beds about such thickness.

[0085]By what thickness is controlled for taking into consideration the carrier mobility and carrier density (decided by ionization potential and electron affinity) of the luminous layer and electron injection transporting bed to combine, or a hole-injection transporting bed. It is possible to design a recombination area and a luminous region freely, and design of the luminescent color, control of the light emitting luminance and the emission spectrum by the cross protection of two electrodes, and control of the spatial distribution of luminescence are enabled.

[0086]The luminous layer of EL element 15 of this invention is made to contain the fluorescence substance which is a compound which has a luminescence function. Metal complex coloring matter, such as tris(8-quinolinolato) aluminum (Alq3) which is indicated by JP,63-264692,A etc. as this fluorescence substance, for example, A blue-green luminescent material which is indicated by JP,6-110569,A (phenyl anthracene derivative), JP,6-114456,A (tetra aryl ethene derivative), JP,6-100857,A, JP,2-247278,A, etc. is mentioned.

[0087]EL element 15 of blue light is good to use for the material of a luminous layer "DMPhen (Triphenylamine)" whose luminous wavelength is about 400 nm. Under the present circumstances, it is preferred that a band gap adopts as an electronic injection layer (Bathocuproine) and a hole injection layer (m-MTDATXA) what is the same material as a luminous layer in order to raise luminous efficiency. It is because an electron remains in an electronic injection layer, an electron hole remains in a hole injection layer, so the recombination of an electron and an electron hole does not happen easily due to a luminous layer only by this using DMPhen with a as large band gap as 3.4 eV for a luminous layer. The luminescent material provided with an amine group like DMPhen is solvable by moving the energy excited in DMPhen to a dopant to the technical problem that structure is unstable and it is hard to extend the life-span of [it], and making light emit from a dopant.

[0088]As an EL material, luminous efficiency can be improved by using a phosphorescence luminescent material. The external quantum efficiency of firefly luminescence material is about 2 to 3%. Since a

phosphorescence luminescent material reaches to about 100% to the firefly luminescence material being 25% in internal quantum efficiency (efficiency which changes the energy by excitation to light), external quantum efficiency becomes high.

[0089]It is good for the host material of the luminous layer of an EL element to use CBP. Here, the phosphorescence luminescent material of red (R) or green (G) blue (B) is doped. All the doped materials contain Ir. R material is good for Btp2Ir (acac) and G material to use 2(ppy)Ir (acac), and for B material to use FIrpic.

[0090]To a hole injection layer and an electron hole transporting bed, for example JP,63-295695,A, JP,2-191694,A, JP,3-792,A, JP,5-234681,A, The various organic compounds indicated in JP,5-239455,A, JP,5-299174,A, JP,7-126225,A, JP,7-126226,A, JP,8-100172,A, and EP0650955A1 grade can be used.

[0091]the above -- it is preferred to use a vacuum deposition method for formation of the hole-injection transporting bed of these, a luminous layer, and an electron injection transporting bed, since a homogeneous thin film can be formed.

[0092](Embodiment 3) It explains hereafter in more detail about the manufacturing method and structure of an EL display panel of this invention. As explained also in advance, TFT11 which drives a pixel to the array substrate 49 is formed first. One pixel comprises four pieces or five TFT(s). Current programming of the pixel is carried out and the programmed current is supplied to EL element 15. Usually, the value by which current programming was carried out is held as a pressure value at the capacitor 19. Pixel configurations, such as combination of this TFT11, are explained later. Next, the picture element electrode 48 as a hole injection electrode is formed in TFT11. The picture element electrode 48 is patternized by photo lithography. In order to prevent the image quality deterioration by a phot conductor phenomena (it is henceforth called contest a phot) generated by carrying out light incidence to the lower layer of TFT11, or the upper layer TFT11, a light-shielding film is formed or arranged.

[0093]What is necessary is to process the surface which forms an organic semiconductor and just to form the electronic thin film using the pentacene molecule which consists of carbon and hydrogen, in order to form TFT in a plastic plate. This thin film possesses sufficient semiconductor characteristic suitable for electron device manufacture while having the crystal grain 20 to 100 times the size of conventional.

[0094]When a pentacene molecule grows on a silicon substrate, it has the tendency to adhere to a surface impurity. For this reason, growing up becomes irregular and it becomes a crystal grain which is too small for manufacturing a quality device. In order to grow up a crystal grain more greatly, it is good to apply first the monolayer "molecule buffer" of the molecule called a cyclohexene on a silicon substrate. In "sticky sites (place which adheres easily)" on silicon, for a wrap reason, this layer can do the clean surface, and it grows up to be even a crystal grain in which a pentacene molecule is very big. A flexible transistor can be mass-produced when it uses at a low temperature, applying the thin film of the big pentacene molecule of such a new crystal grain.

[0095]It may heat and semiconductor membrane may be formed, after forming in island shape the metal thin film which serves as a gate on a substrate and vapor-depositing or applying an amorphous silicon film on this. Semiconductor membrane crystallizes good into the portion formed in island shape. Therefore, mobility becomes good.

[0096]As an organic transistor (TFT), it is preferred to adopt the structure called a static induction transistor (SIT), and it uses pentacene of an amorphous state. The mobility of an electron hole is lower than $1x10-cm^2/Vs$ and the crystallized pentacene. However, a frequency characteristic can be improved by adopting SIT structure. The thickness of pentacene has preferred not less than 100-nm thing set to 300 nm or less.

[0097]A P type field effect transistor may be sufficient as organic TFT, and TFT can be formed on a plastic plate. In this case, as for the pentacene which can constitute a flexible TFT type display panel, since it is possible to bend the whole plastic plate, it is preferred to consider it as a polycrystalline state. It is preferred to use PMMA for the material of gate dielectric film.

[0098]If oxygen plasma and O_2 Usher are used at the time of washing, ashing also of the smoothing film 71 of the periphery of the picture element electrode 48 will be carried out simultaneously, and the periphery of the picture element electrode 48 will be scooped out. In order to solve this technical problem, as drawing 4 shows, by this invention, the edge protective film 81 which becomes a periphery of the picture element electrode 48 from an acrylic resin is formed. As a component of the edge protective film 81, the organic materials and the identical materials which constitute the smoothing film 71, such as acrylic resin and polyimide resin, are illustrated, in addition inorganic materials, such as SiO_2 and SiNx, $aluminum_2O_3$, etc. are illustrated.

[0099]The edge protective film 81 is formed so that after patterning of the picture element electrode 48 and between the picture element electrode 48 may be filled. Of course, it cannot be overemphasized that it is good also as a bank (spacer keep a metal mask from touching the picture element electrode 48 directly) of the metal mask at the time of forming this edge protective film 81 in not less than 2-micrometer a height of 4 micrometers or less, and distinguishing organic electroluminescence material by different color with.
[0100]A vacuum evaporator uses the device which converted the commercial high vacuum evaporation apparatus (the Japan vacuum-technology incorporated company make, EBV-6DA type). the main exhaust is a turbo-molecular pump (Makoto Osaka fictitious stock type company make, TC1500) of 1500 l. of exhaust speeds / min -- a ultimate vacuum -- about -- it is below $1x10e^{-6}$Torr (Pa), and all the vacuum evaporation is performed in the range of 2 - $3x10e^{-6}$Torr (Pa). All the vacuum evaporation is good to carry out by connecting DC power supply (Kikusui electronic incorporated company make, PAK10-70A) to the resistance heating type deposition boat made from tungsten.
[0101]Thus, on the array substrate arranged in a vacuum layer, 20-50 nm of carbon films are formed. Next, a 4-(N,N-bis(p-methylphenyl)amino)-alpha-phenylstilbene is formed in about 5 nm of thickness with the evaporation rate of 0.3 nm/s as a hole injection layer.
[0102]As an electron hole transporting bed, N,N'-bis(4'-diphenylamino 4-biphenylyl)-N,N'-diphenylbenzidine (made by Hodogaya chemicals incorporated company), Vapor codeposition of the 4-N,N-diphenylamino alpha-phenylstilbene is carried out with the evaporation rate of 0.3 nm/s and 0.01 nm/s, respectively, and it is formed in about 80 nm of thickness.
[0103]as a luminous layer (electron transport layer), tris(8-quinolinolato) aluminum (said -- Renhua -- study incorporated company make) is formed in about 40 nm of thickness with the evaporation rate of 0.3 nm/s.
[0104]next -- as an electron injection electrode -- an aluminum-Li alloy (high grade chemicals incorporated company make.) Only Li is formed in about 1 nm of thickness with the evaporation rate of about 0.1 nm/s at low temperature from the aluminum/Li weight ratios 99/1, Then, temperature up of the aluminum-Li alloy was carried out further, and from the state in which Li was all out, only aluminum was formed in about 100 nm of thickness with the evaporation rate of about 1.5 nm/s, and was used as the electron injection electrode of a lamination type.
[0105]Thus, after the created organic thin film EL element leaked the inside of a vacuum evaporation tub with dry nitrogen, under a dry nitrogen atmosphere, it stuck the Corning 7059 glass closure lid 41 by the sealing compound 45 (the Anelva [CORP.] make, a trade name: super back seal 953-7000), and used it as the display panel. The drier 55 is arranged in the space of the closure lid 41 and the array substrate 49. Since the organic electroluminescence film is weak to humidity, this absorbed the moisture which permeates the sealing compound 45 with the drier 55, and has prevented degradation of the organic electroluminescence layer 47.
[0106]In order to control osmosis of the moisture from the sealing compound 45, it is a good measure to lengthen the course (path) from the outside. For this reason, the detailed crevice 43 and the heights 44 are formed in the periphery of a viewing area in the display panel of this invention. The heights 44 formed in the periphery of the array substrate 49 are formed doubly at least. As for the interval (formed pitch) of a convex and a convex, to not less than 100 micrometers 500 micrometers or less, it is preferred again that the height of a convex shall be not less than 30 micrometers 300 micrometers or less. These heights are formed with the La Stampa art. The method which OMRON Corp. has adopted as a micro-lens formation method, and the method which Matsushita Electric uses as a formation method of a microlens with the pickup lens of CD are applied to this La Stampa art.
[0107]On the other hand, the crevice 43 is formed also in the closure lid 41. The formed pitch of the crevice 43 is made the same as that of the formed pitch of the heights 44. Thus, the heights 44 get into the crevice 43 exactly by making a formed pitch the same, and a position gap does not occur between the closure lid 41 and the array substrate 49 at the time of manufacture of a display panel. The sealing compound 45 is arranged between the crevice 43 and the heights 44. The sealing compound 45 prevents permeation of the moisture from the outside while pasting up the closure lid 41 and the array substrate 49.

[0108]As for using what consists of acrylic resin with UV (ultraviolet rays) hardening type as the sealing compound 45, and an acrylic resin, it is preferred to use what has a fluorine group. In addition, the adhesives or the binder of an epoxy system may be used. As for the refractive index of adhesives or a binder, it is preferred to use or more 1.47 1.54 or less thing. As for especially seal adhesives, it is preferred

that impalpable powder, such as impalpable powder of titanium oxide and silicon oxide, shall be added at a rate of 95% or less not less than 65% by a weight ratio, and the average diameter of the particle diameter of this impalpable powder shall be not less than 20 micrometers 100 micrometers or less. This is because the effect which controls penetration of the humidity from the forge-fire outside where the weight ratio of impalpable powder increases becomes high. However, if too large, air bubbles etc. will enter easily, space will become large on the contrary, and a sealing effect will fall.

[0109]Especially the weight of a drier has desirable 0.06g or more thing set to 0.15g or less 0.04g or more per 10 mm in length of seal 0.2g or less. When this has too little quantity of a drier, it is for a moisture preventive effect to fade and for an organic electroluminescence layer to deteriorate immediately. Conversely, if too large, when a drier carries out a seal, it becomes an obstacle, and a good seal cannot be performed.

[0110]Although it is the composition closed using the closure lid 41 of glass in drawing 2, it may be closure using a film like drawing 5. For example, using for the film of an electrolytic condenser what vapor-deposited DLC (diamond- -like carbon) as a sealing film is illustrated.Moisture perviousness is very bad (moisture proof) one, and can use this film as the sealing film 73. The composition which vapor-deposits a DLC film directly on the surface of the transparent electrode 72 may be used. The thickness of a thin film is n-d (n synthesizes and (n-d of each thin film is calculated) calculates those refractive indicees, when the refractive index of a thin film and two or more thin films are laminated.). d synthesizes and calculates those refractive indicees, when the thickness of a thin film and two or more thin films are laminated. It is good to make it below the luminescence dominant wavelength lambda of EL element 15 become. By fulfilling this condition, the optical extraction efficiency from EL element 15 more than doubles as compared with the case where it closes with a glass substrate. The alloy, the mixture, or laminated material of aluminum and silver may be formed.

[0111]It is reflected with the reflection film 46, and the half of the light generated from the organic electroluminescence layer 47 penetrates the array substrate 49, and is emitted. However, since outdoor daylight is reflected, a reflect lump occurs, and the reflection film 46 reduces display contrast. For this measure, the lambda/4 board 50 and the polarizing plate 54 are arranged to the array substrate 49. When a pixel is a reflector, the light generated from the organic electroluminescence layer 47 is emitted upward. Therefore, the lambda/4 board 50 and the polarizing plate 54 must be arranged at the optical outgoing radiation side. A reflection type pixel is obtained by constituting the picture element electrode 48 from aluminum, chromium, silver, etc. An interface with the organic electroluminescence layer 47 becomes large by providing heights (or uneven part) in the surface of the picture element electrode 48, an emission area becomes large, and luminous efficiency improves.

[0112]Between the array substrate 49 and the polarizing plate (polarization film) 54, one sheet or two or more phase films (a phase plate, a phase rotating means, a phase difference plate, a phase difference film) are arranged. It is preferred to use polycarbonate as a phase film. This phase film generates phase contrast for incident light to emitted light, and contributes to performing light modulation efficiently.

[0113]In addition, an organic resin board or organic resin films, such as polyester resin, PVA resin, polysulphone resin, vinylchloride resin, ZEONEX resin, an acrylic resin, and polystyrene resin, etc. may be used as a phase film. In addition, the crystal of crystal etc. may be used. The phase contrast of one phase plate has preferred not less than 50-nm thing set to 350 nm or less and not less than 80 more nm 220 nm or less to 1 shaft orientations.

[0114]The circular light board 74 (circular light film) which unified the phase film and the polarizing plate may be used so that it may illustrate to drawing 5.

[0115]It is preferred for a color or paints to color the lambda/4 board (phase film) 50, and to give the function as a light filter. Since the red (R) purity of especially an organic electroluminescence layer is bad, the fixed wavelength range is omitted with the lambda/4 colored board 50, and a color temperature is adjusted. As for a light filter, it is common to be provided by pigment dispersion type resin as a dyeing filter, and these paints absorb the light of a specific wavelength band region, and penetrate the light of the wavelength band region which was not absorbed.

[0116]As mentioned above, a part or the whole of a phase film may be colored, or a diffusing function may be given to the whole in part. Embossing of the surface may be carried out or an antireflection film may be formed for acid resisting. It is preferred to form a light-shielding film or a light absorption film in a part without the part or trouble which is not effective in image display, and to tighten the black level of a display image, or to demonstrate the contrast improvement effect by antihalation. A micro lens may be formed in the shape of boiled fish paste, or matrix form by forming unevenness in the surface of a phase film. A micro lens is arranged so that it may correspond to one picture element electrode or a trichromatic pixel,

respectively.
[0117]Although described also in advance, since phase contrast can be generated by rolling or photopolymerization at the time of formation of a light filter, the function of a phase film may be given to a light filter. In addition, phase contrast may be given by carrying out photopolymerization of the smoothing film 71 of drawing 5. If constituted in this way, it becomes unnecessary not to constitute a phase film or to arrange it out of a substrate, and the composition of a display panel also becomes simple and can desire low cost-ization. The above matter is applicable also to the polarizing plate 54.
[0118]The thing of the resin film in which the polarizing plate 54 added iodine etc. to poly vinyl alcohol (PVA) resin is illustrated. Since the polarizing plate of the polarization separating means of a couple performs polarized light separation by absorbing the polarization component of the specific direction of a polarization axis, and a different direction among incident light, its utilization efficiency of light is comparatively bad. Then, the reflecting polarizer which performs polarized light separation may be used by reflecting the polarization component (reflective polarizer: reflective polarizer) of the specific direction of a polarization axis, and a different direction among incident light. If constituted in this way, the utilization efficiency of light will increase with a reflecting polarizer, and a display brighter than the above-mentioned example using a polarizing plate will be attained.
[0119]Besides such a polarizing plate or a reflecting polarizer, as a polarization separating means of this invention, It is also possible to use what combined the cholesteric liquid crystal layer and lambda (1/4) board, the thing divided into reflective polarization and transmitted polarized light using Brewster's angle, the thing using a hologram, a polarization beam splitter (PBS), etc.
[0120]The AIR coat is given to the surface of the polarizing plate 54 although not illustrated in drawing 2.
[0121]Although TFT is connected to the picture element electrode 48, it is not limited to this. To an active matrix, a barista, a thyristor, a diode method (TFD), ring-die oared besides a thin film transistor (TFT), a photo-diode, a photo transistor, FET, a MOS transistor, and a PLZT element are also possible as a switching element. That is, what constitutes a switching element and a driver element can use these either.

[0122]It is preferred to adopt LDD (low doping drain) structure as TFT. All the general element which carry out transistor operation of switching, such as FET, etc. is meant in TFT. The composition of EL film, panel structure, etc. are applicable also to a simple matrix type display panel. On these specifications, although an organic EL device (OEL, PEL, PLED, OLED) is mentioned as an example and explained as an EL element, it is not limited to this, and it is applied also to an inorganic EL element.
[0123]the active matrix system used for an organic electroluminescence display panel -- (1) -- a specific pixel must be chosen and two conditions that required display information can be given and that current can be sent through an EL element through (2) 1 frame period must be fulfilled.
[0124]In order to fulfill these two conditions, in the element composition of the conventional organic electroluminescence shown in Drawing 220, the thin film transistor for switching for 1st TFT11a to choose a pixel and 2nd TFT11b are taken as the thin film transistor for a drive for supplying current to EL element 15.
[0125]Although TFT11a for switching is required for liquid crystals as compared with the active matrix system used for a liquid crystal here, TFT11b for a drive is required in order to make EL element 15 turn on. As this reason, in the case of a liquid crystal, although an ON state can be held by impressing voltage, it is because the lighted condition of the pixel 16 cannot be maintained if it does not continue sending current when it is EL element 15.
[0126]Therefore, in order to continue sending current, making TFT11b for a drive one [an organic electroluminescence display panel] must be continued. First, if both a scanning line and the data line are turned on, an electric charge will be accumulated in the capacitor 19 through TFT11a for switching. The one [current continues flowing from the current supply source line 20, and / the pixel 16] over 1 frame period in order that this capacitor 19 may continue applying voltage to the gate of TFT11b for a drive, even if TFT11a for switching is come by off.
[0127]When displaying gradation using this composition, it is necessary to impress the voltage according to gradation as gate voltage of TFT11b for a drive. Therefore, dispersion in the ON state current of TFT11b for a drive appears in a display as it is.
[0128]If the ON state current of a transistor is the transistor formed with the single crystal, it is very uniform, but. In the low-temperature polycrystal transistor which the forming temperature which can be formed in a cheap glass substrate formed with the low-temperature-polysilicon art of 450 degrees or less. Since it has dispersion in the threshold in **0.2V - 0.5V, the ON state current which flows through TFT11b for a drive varies corresponding to this, and unevenness occurs in a display. Such unevenness generates

not only dispersion in threshold voltage but the mobility of TFT and the thickness of gate dielectric film. The characteristic changes also with degradation of TFT11.
[0129]Therefore, in order to obtain a uniform display, it is necessary to control the characteristic of a device by the method of displaying gradation in analog, strictly, and the spec. of suppressing this dispersion within a prescribed range cannot be filled with it at the present low-temperature polycrystal poly-Si TFT. Since this problem is solved, four transistors are provided in 1 pixel and how to make dispersion in threshold voltage compensate by a capacitor, and to acquire uniform current, the method of forming a current regulator circuit for every pixel, and attaining equalization of current, etc. can be considered.
[0130]However, since the current by which these methods are programmed is made through EL element 15, when a current route changes, the transistor which controls driving current serves as a source follower to the switching transistor connected to a power source line, and a drive margin becomes narrow. Therefore, it will have the technical problem that driver voltage becomes high.
[0131]It is necessary to use the switching transistor linked to a power supply in the field where impedance is low, and the technical problem that it is influenced by the characteristic fluctuation of EL element 15 also has this working range. When kink current moreover occurs in the volt ampere characteristic in a saturation region, or when change of the threshold voltage of a transistor occurs, the technical problem that the memorized current value is changed also occurs.
[0132]Even if TFT11 which controls the current which flows into EL element 15 does not become source follower composition to an aforementioned problem and the EL element structure of this invention has kink current in the transistor, It is the composition which can make small change of the current value which can suppress the influence of kink current to the minimum, and is memorized.
[0133]The EL element structure of this invention is specifically formed of two or more TFT11 and EL element 15 which a unit pixel becomes from at least four, as shown in drawing 6 (a). A picture element electrode is constituted so that it may lap with a source signal line. That is, the smoothing film which consists of an insulator layer or acrylic material is formed on the source signal line 18, it insulates, and a picture element electrode is formed on this insulator layer. Thus, the composition which piles up a picture element electrode is called a high aperture (HA) structure on the source signal line 18.
[0134]The 1st gate signal line (the 1st scanning line) 17a being active (ON voltage is impressed) and by carrying out, It lets 1st TFT(or switching element) 11a and 3rd TFT(or switching element)11c pass, 2nd TFT11b opens the 1st gate signal line 17a by that it is active (ON voltage is impressed) and carrying out so that the current value which should be passed to said EL element 15 may be passed and between the gate of 1st TFT11a and a drain may be short-circuited, and. It is remembered that the gate voltage (or drain voltage) of 1st TFT11a passes said current value to the capacitor 19 connected between the gate of 1st TFT11a, and sauce.
[0135]As for the capacitor 19 which is the sauce inter gate capacity of 1st TFT11a, it is preferred to consider it as the capacity of 0.2 pF or more. There is also an example which forms the capacitor 19 separately as other composition. That is, this is composition which forms storage capacitance from a capacitor electrode layer, gate dielectric film, and a gate metal. It is more desirable to constitute a capacitor from the viewpoint which prevents the brightness lowering by leak of the M3 transistor 11c, and a viewpoint for stabilizing a display action separately in this way. The size of the capacitor 19 has good 0.4-pF or more thing set to 1.2 pF or less also of 0.2 pF or more in in 2 pF or less.
[0136]As for the capacitor 19, it is preferred to be formed in the non display regions between the adjoining pixels. When creating a full color organic electroluminescence layer generally, in order to form an organic electroluminescence layer by the mask deposition by a metal mask, a mask position gap occurs in the formation position of an organic electroluminescence layer, and there is a danger that the organic electroluminescence layer of each color will lap. Therefore, not less than 10 micrometers of non display regions between the pixels which each color adjoins must be left, and this portion turns into a portion which does not contribute to luminescence. Therefore, it becomes an effective means for the improvement in a numerical aperture to form the capacitor 19 in this field.
[0137]Next, the 2nd gate signal line 17b is activated, using the 1st gate signal line 17a as inactive (OFF voltage is impressed), It operates so that it may change to the course containing the 4th TFT11d and said EL element 15 by which the course into which current flows was connected to 1st [said] TFT11a and EL element 15 and the memorized current may be sent through said EL element 15.
[0138]This circuit has four TFT11 in 1 pixel, and the gate of the 1st transistor M1 is connected to the sauce of the 2nd transistor M2, The gate of the 2nd transistor M2 and the 3rd transistor M3 to the 1st gate signal line 17a. The drain of the 2nd transistor M2 is connected to the sauce of the 3rd transistor M3, and the sauce of the 4th transistor M4, and the drain of the 3rd transistor M3 is connected to the source

signal line 18. The gate of the 4th transistor M4 is connected to the 2nd gate signal line 17b, and the drain of the 4th transistor M4 is connected to the anode electrode of EL element 15.

[0139]P channel constitutes all the TFT(s) from drawing 6. Somewhat, although mobility is low as compared with TFT of N channel, since pressure-proofing does not generate degradation easily greatly again, either, P channel is preferred. However, it is not limited only to this invention constituting EL element composition from a P channel. It may constitute only from an N channel and may constitute using both N channel and P channel (see drawing 74, Drawing 126, Drawing 127, etc.).

[0140]The 3rd and 4th transistors are constituted from same polarity, and it constitutes from an N channel, and, as for the 1st and 2nd transistors, constituting from a P channel is preferred. Generally P channel transistor is compared with N channel transistor, There are the features, like reliable there is little kink current, and to the EL element which obtains the target luminescence intensity by controlling current, if 1st TFT11a is used as P channel, an effect will become large.

[0141](Embodiment 4) The EL element composition of this invention is hereafter explained using drawing 7. The EL element composition of this invention is controlled by two timing. The 1st timing is timing which makes a required current value memorize. When TFT11b and TFT11c turn on to this timing, it becomes drawing 7 (a) as an equivalent circuit. The predetermined current I1 is written in from a signal wire here, TFT11a will be in the state where the gate and the drain were connected, and the current I1 will flow through it through this TFT11a and TFT11c. Therefore, the voltage between the gate sauce of TFT11a is set to V1 so that the current I1 may flow.

[0142]TFT11a and TFT11c close the 2nd timing, it is the timing which TFT11d opens and the equivalent circuit at that time serves as drawing 7 (b). In this case, the TFT11a of M1 becomes constant [the current I1] in order to always operate in a saturation region, and the voltage V1 between the sauce gates of TFT11a becomes [being held with as, and].

[0143]The gate of TFT11a and the gate of TFT11c are connected to the same gate signal line 17a. However, the gate of TFT11a and the gate of TFT11c may be connected to the different gate signal line 17b (it enables it to control SA1 and SA2 individually). That is, a 1-pixel gate signal line becomes three (the composition of drawing 6 is two). By controlling individually the ON/OFF timing of the gate of TFT11a, and the ON/OFF timing of the gate of TFT11c, current value dispersion of EL element 15 by dispersion in TFT11 can be reduced further.

[0144]The 1st gate signal line 17a and 2nd gate signal line 17b are carried out in common, and if the 3rd and 4th transistors are used as a different conductivity type (N channel and P channel), simplification of a drive circuit and the numerical aperture of a pixel can be raised. If constituted in this way, as operation timing of this invention, the write-in course from a signal wire will be come by off. That is, if the course into which current flows has branching when predetermined current is memorized, an exact current value will not be memorized by the sauce inter gate capacity (capacitor) of M1. The 3rd transistor M3 and 4th transistor M4 are used as different conducted type of current, and M4 is enabled one after M3 certainly turns off to the timing from which a scanning line changes by controlling a mutual threshold. However, since it is necessary to control a mutual threshold correctly in this case, the cautions to a process are required.

[0145]Although the circuit described above is realizable with at least four transistors, For Miller-effect reduction, as shown in drawing 6 (b), cascade connection of the TFT11e (M5) is carried out, and the principle of operation is the same as for four or more in the total of a transistor so that more exact timing may control or mention later. Thus, the current programmed via the 3rd transistor M3 can be sent now through EL element 15 with more sufficient accuracy by having composition which added TFT11e.

[0146]In the composition of drawing 6, it is still more preferred that the current value Ids in the saturation region of 1st TFT11a fulfills the conditions of a lower type. In a lower type, the value of lambda fulfills or more 0.01 0.06 or less conditions between the adjoining pixels.

[0147]$Ids=k*(Vgs-Vth)^2 (1+ Vds*lambda)$

In this invention, although the working range of TFT11a is limited to a saturation region, it separates from the transistor characteristics in a saturation region from the ideal characteristic, and is generally influenced by the voltage between sauce drains (Miller effect).

[0148]The case where the shift of the threshold which is set to each TFT11a in the adjoining pixel as for deltaVt occurs is considered. In this case, the current value memorized is the same. If the shift of a threshold is set to deltaL, abbreviation delta Vxlambda is equivalent to a gap of the current value of EL element 15 by changing the threshold of TFT11a. Therefore, in order to suppress a gap of current below to x (%), it turns out as y(V) that lambda must be below 0.01xx/y between the pixels which adjoin the permissible dose of a shift of a threshold. This acceptable value changes with the luminosity of application.

If the amount of change has not less than 2% of luminosity in the brightness area to 100 cd/m^2 - 1000 cd/m^2, human being will recognize the changed boundary line. Therefore, it is required for the amount of change of luminosity (current amount) to be less than 2%. When luminosity is higher than 100 cd/cm^2, the luminance variation of the adjoining pixel will be not less than 2%. When using EL display device of this invention as a display for personal digital assistants, the demand luminosity is a 100-cd[/m] ^{2} grade. When the pixel configuration of drawing 6 was made as an experiment and change of the threshold was actually measured, in TFT11a of the adjoining pixel, it turned out that the maximum of change of a threshold is 0.3V. Therefore, in order to suppress change of luminosity within 2%, lambda must be 0.06 or less. However, since human being cannot recognize change, it is not necessary to carry out to 0.01 or less. In order to attain dispersion in this threshold, it is necessary to enlarge transistor size enough, and it is unreal.

[0149]It is preferred to be constituted so that the current value Ids in the saturation region of 1st TFT11a may fill a lower type. Change of lambda is made into 5% or less 1% or more between the adjoining pixels.

[0150]Ids=k*(Vgs-Vth) ^{2} (1+ Vds*lambda)

If lambda of the above-mentioned formula has change even when change of a threshold does not exist even if between the adjoining pixels, the current value which flows through an EL element will be changed. In order to suppress change within **2%, change of lambda must be suppressed to **5%. However, since human being cannot recognize change, it is not necessary to make it to 1% or less. In order to attain 1% or less, it is necessary to enlarge transistor size fairly, and it is unreal.

[0151]According to an experiment, an array trial production, and examination, it is preferred that not less than 10 micrometers 200 micrometers or less of channel length of 1st TFT11a shall be not less than 15 micrometers 150 micrometers or less further. This is considered to be because for an electric field to be eased and for a kink effect to be low suppressed, when the grain boundaries included in a channel increase in number when channel length L is lengthened.

[0152]TFT11 which constitutes a pixel is formed by the poly-Si TFT formed by the laser recrystallization method (laser annealing), and it is preferred that the direction of the channel in all the transistors is the same direction to the direction of radiation of laser.

[0153]Dispersion in transistor characteristics proposes the circuitry which does not affect a display, and four or more transistors are [therefore] required for the purpose of this invention. If the characteristic of four transistors does not gather when these transistor characteristics determine a circuit constant, it is difficult to ask for a suitable circuit constant. To the major axis direction of laser radiation, by the case where the direction of a channel is level, and the case of being vertical, the threshold and mobility of transistor characteristics differ from each other, and are formed. The grade of dispersion is the same in both cases. Since the average value of mobility and a threshold differs horizontally if perpendicular, the same one of the direction of a channel of all the transistors which constitute a pixel is desirable.

[0154]When Cs and the OFF state current value of 2nd TFT11b are set to Ioff for the capacity value of the capacitor 19, it is preferred to fill a following formula.

[0155]It is preferred to fill a following formula preferably to 3<Cs/Ioff<24 pan.

[0156]By setting the OFF state current of 6<Cs/Ioff<18TFT11b to 5 or less pA, it is possible to suppress change of the current value which flows through an EL element to 2% or less. This is because the electric charge stored between gate sauce (both ends of a capacitor) in the voltage non-writing state cannot be held between 1 fields, when leakage current increases. Therefore, if the capacity for accumulation of the capacitor 19 is large, the permissible dose of the OFF state current will also become large. Change of the current value between adjacent pixels can be suppressed to 2% or less by filling said formula.

[0157]It is preferred that the transistor which constitutes an active matrix is constituted by the p-ch polysilicon thin film transistor, and TFT11b is made into the multi-gate structure which is beyond dual gate structure. In order that TFT11b may act as a switch between the sauce drains of TFT11a, the characteristic that an ON/OFF ratio is high as much as possible is required. In order to fill this demand, the high characteristic of an ON/OFF ratio can be realized by making structure of the gate of TFT11b into multi-gate structure.

[0158]The transistor which constitutes an active matrix comprises a polysilicon thin film transistor, and it is preferred that below 54-micrometer^2 carries out (channel width W) * (channel length L). [of each transistor] (Channel width W) * (channel length L) and dispersion of transistor characteristics have correlation. The cause of dispersion in transistor characteristics has many things resulting from dispersion in the energy by the exposure of laser, etc., and in order to absorb this, it is desirable to consider it as the structure which contains many exposure pitches (generally about ten micrometers) of laser by the inside of

a channel as much as possible. Then, by below 54-micrometer^2 carrying out (channel width W) * (channel length L), there is no dispersion resulting from laser radiation, and the thin film transistor to which the characteristic was equal can be obtained. [of each transistor] Since characteristic dispersion by area will occur if transistor size becomes small too much, As for (channel width W) * (channel length L), it is [more than 9 micrometer^2] still more preferred to make it below 45-micrometer^2 become [more than 16 micrometer^2]. [of each transistor]

[0159]It is preferred to make mobility change of 1st TFT11a in the adjoining unit pixel 20% or less. It is because capacity between the gate sauce of the 1st transistor M1 cannot be charged by the time the charging capacity of a switching transistor deteriorates and it passes a current value required for within a time, when mobility runs short. Therefore, dispersion in the luminosity between pixels can be made below into ****** by suppressing dispersion in movement within 20%.

[0160]As mentioned above, although drawing 6 was explained as a pixel configuration, these are applicable also to the composition illustrated to drawing 8 and drawing 9. Hereafter, pixel configurations, such as drawing 8, are explained.

[0161]When setting up the current sent through EL element 15, voltage between gate sauce which produces the signal current sent through TFT11a for conversion in Iw, as a result TFT11a for conversion is set to Vgs. Since between the gate drains of TFT11a for conversion has connected too hastily by TFT11d at the time of writing, the TFT11a for conversion operates in a saturation region. Therefore, the signal current Iw is given by the following formulas.

[0162]

(Several 1) Iw=mu1, Cox1andW1/L1/-- 2 (Vgs-Vth1) ^{2}, Cox of here is the gate capacitance per unit area, and is given by Cox=epsilon 0 and epsilonr/d. The mobility of a career and W show channel width, L shows channel length, as for the threshold and mu which are TFT as for Vth, vacuous mobility and epsilonr show the specific inductive capacity of gate dielectric film, as for epsilon 0, and d is the thickness of gate dielectric film.

[0163]A current level will be controlled by TFT11b for a drive by which Idd is connected in series with EL element 15 if the current which flows into EL element 15 is set to Idd. In this invention, since the voltage between the gate sauce is in agreement with Vgs of a formula (several 1), if it assumes that the TFT11b for a drive operates in a saturation region, the following formulas will be realized.

[0164]

(Several 2) Generally conditions for the thin film transistor (TFT) of Cox2 and Idrv=mu 2 and W2/L2 / 2 (Vgs-Vth2) ^{2} insulated-gate electric field effect type to operate in a saturation region are given by the following formulas by making Vds into the voltage between drain sauce.

[0165]

(Several 3) |Vds|>|Vgs-Vth| -- here, since the inside of a small pixel is approached and it is formed, TFT11a for conversion and TFT11b for a drive are profile mu1=mu2 and Cox1=Cox2, and unless creativity in particular is put, they are considered to be Vth1=Vth2. Then, the following formulas are easily drawn from a formula and (several 2) a formula at this time (several 1).

[0166]

(Several 4) Idrv/Iw=(W2/L2)/(W1/L1)

Although it is common in a formula (several 1) and (several 2) a formula to vary for every pixel, every product, or every manufacture lot as for the value of mu, Cox, and Vth itself, the point which it should be careful of here, (Several 4) Since a formula does not contain these parameters, I hear that it is not dependent on these dispersion, and there is a value of Idrv/Iw. The driving current Idd which Idrv/Iw=1, i.e., Iw and Idrv, will become the same value, and will flow into EL element 15 temporarily if it designs with W1=W2 and L1=L2, Since it is not based on characteristic dispersion of TFT but becomes the same as that of the signal current Iw correctly, the light emitting luminance of EL element 15 is correctly controllable as a result.

[0167]As mentioned above, since it is fundamentally the same, if the signal level of a cutoff level is impressed to the gate in the common electric potential in both TFT(s), threshold Vth1 of TFT11a for conversion, and threshold Vth2 of TFT11b for a drive, Both TFT11a for conversion and TFT11b for a drive must be in non-switch-on. However, Vth2 may become low rather than Vth1 by factors, such as dispersion in a parameter, also within a pixel actually. Since the leakage current of subthreshold level flows into TFT11b for a drive at this time, EL element 15 presents fine luminescence. The contrast of a screen falls by this fine luminescence, and display properties are spoiled.

[0168]Especially in this invention, it has set up so that threshold voltage Vth2 of TFT11b for a drive may

not become lower than threshold voltage Vth1 of TFT11a for conversion corresponding within a pixel. For example, even if gate length L2 of TFT11b for a drive is made longer than the gate length L1 of TFT11a for conversion and it changes the process parameter of these thin film transistors, it is able to keep Vth2 from becoming lower than Vth1, and to control very small current leakage. The above matter is applied also to the relation between TFT11a for conversion of drawing 6, and TFT11d.
[0169]TFT11b for a drive etc. which control the driving current which flows into the light emitting device which consists of TFT11a for conversion into which signal current flows, and EL element 15 grade as shown in drawing 8. TFT11c for taking in which connects or intercepts a pixel circuit and data-line data by control of the 1st scanning line scanA (SA), TFT11d for switching which writes in by control of the 2nd scanning line scanB (SB), and short-circuits between the gate drains of TFT11a for conversion during a period, It comprises EL element 15 as the capacitor 19 and a light emitting device for after a write end to hold the voltage between gate sauce of TFT11a for conversion, etc. Thus, the gate signal line can apply the composition of the whole specification of this invention based on drawing 6 etc. which were mentioned above, a function, operation, etc. from their being each two pixels.
[0170]Although, as for TFT11c for taking in in drawing 8, the transistor of N-channel MOS (NMOS) and others comprises a P channel MOS (PMOS), this needs to be an example and does not necessarily need to be this passage. Although the terminal of one of these is connected to the gate of TFT11a for conversion and the terminal of another side is connected to Vdd (power supply potential), constant potential not only Vdd but arbitrary may be sufficient as the capacitor 19. The cathode (negative pole) of EL element 15 is connected to earth potentials. Therefore, it cannot be overemphasized that the above matter is applied to drawing 6 etc.
[0171]The terminal voltage of EL element 15 changes also with temperature. Usually, it becomes low as it is high and temperature becomes high, when temperature is low. This tendency has a linear relation. Therefore, it is preferred to adjust Vdd voltage with an outside temperature (correctly temperature of EL element 15). A temperature sensor detects an outside temperature, feedback of a Vdd voltage generation section is applied, and Vdd voltage is changed. Vdd voltage is Centigrade 10 ** change, and it is preferred to consider it as 6% or less not less than 3% especially 8% or less not less than 2%.
[0172]As for Vdd voltage, such as drawing 6, it is preferred to make it lower than the OFF state voltage of TFT11. Specifically, Vgh (OFF state voltage of a gate) should be made higher than Vdd-0.5V at least. When lower than this, off-leak of TFT occurs and the shot unevenness of laser annealing comes to be conspicuous. Since the amount of off-leaks will increase conversely if too high, it should be made lower than Vdd+4V. Therefore, below or more [-0.5] V+4V should make still more preferably OFF state voltage Vgh of the gate, i.e., the Vdd power supply voltage in drawing 6, less than more than 0V+2V, and it is made for the OFF state voltage of TFT impressed to a gate signal line to be enough come by off. As for Vgl, since Vgl serves as OFF state voltage when TFT is N channel, it is preferred to make it or more [-4] Vbelow 0.5V become a range not more than more than -2V0V further to GND voltage.
[0173]As mentioned above, although the pixel configuration of the current programming of drawing 6 was described, it cannot be overemphasized that it is not limited to this and can apply also to the pixel configuration of voltage programs, such as drawing 74 and drawing 76. As for Vt offset cancellation of a voltage program, it is preferred to compensate every R, G, and B individually.
[0174]The composition of drawing 8 is provided with the following.
The scanning line driving circuit which chooses the scanning lines scanA and scanB one by one.
The data line driving circuit containing current source CS which generates the signal current Iw which has a current level according to brightness information, and is supplied to data-line data one by one.
Two or more pixels containing current drive type EL element 15 which is allotted to the intersection of each scanning lines scanA and scanB and each data-line data, and emits light in response to supply of driving current.

[0175]The accession department (specifically, it comprises TFT11c for taking in) into which the pixel configuration shown in drawing 8 as feature items incorporates the signal current Iw from the data-line data concerned when the scanning line scanA concerned is chosen, It consists of a converter which once transforms the current level of the incorporated signal current Iw into a voltage level, and holds it, and an actuator which sends the driving current which has a current level according to the held voltage level through the light emitting device OLED concerned (it may otherwise be called EL, OEL, PEL, and PLED for short).
[0176]Said converter contains TFT11a for conversion provided with a gate, sauce, the drain, and the channel, and the capacitor 19 linked to the gate. A gate is made to generate the voltage level which sent

through the channel the signal current Iw incorporated by TFT11a for conversion, and the accession department, and was changed, and the voltage level produced to the capacitor 19 is held.
[0177]Said converter contains TFT11d for switching inserted between the drain of TFT11a for conversion, and the gate. TFT11d for switching flows, when transforming the current level of the signal current Iw into a voltage level, the drain and gate of TFT11a for conversion are electrically connected, and the gate of TFT11a for conversion is made to produce the voltage level on the basis of sauce. TFT11d for switching is intercepted when holding a voltage level to the capacitor 19, and it separates the capacitor 19 linked to the gate of TFT11a for conversion, and this from the drain of TFT11a for conversion.
[0178]Said actuator contains TFT11b for a drive provided with a gate, a drain, sauce, and a channel. TFT11b for a drive accepts in a gate the voltage level held at the capacitor 19, and the driving current which has a current level according to it flows into EL element 15 via a channel. Direct continuation of the gate of TFT11a for conversion and the gate of TFT11b for a drive is carried out, and he constitutes a current mirror circuit, and is trying for the current level of the signal current Iw and the current level of driving current to serve as proportionality.
[0179]The TFT11b for a drive operates in a saturation region, and sends through EL element 15 the driving current according to the difference of the voltage level and threshold voltage which were impressed to the gate.
[0180]TFT11b for a drive is set up so that the threshold voltage may not become lower than the threshold voltage of TFT11a for conversion corresponding within a pixel. Specifically, TFT11b for a drive is set up so that the gate length may not become shorter than the gate length of TFT11a for conversion. Or TFT11b for a drive may be set up so that the gate dielectric film may not become thinner than the gate dielectric film of TFT11a for conversion corresponding within a pixel.
[0181]TFT11b for a drive adjusts the impurity concentration poured into the channel, and it may be set up so that threshold voltage may not become lower than the threshold voltage of TFT11a for conversion corresponding within a pixel. As for TFT11a for conversion, and TFT11b for a drive, both should be turned off, if the signal level of a cutoff level is impressed to the gate of both the thin film transistors by which common connection was carried out when it sets up temporarily so that the threshold voltage of TFT11a for conversion and TFT11b for a drive may become the same. However, dispersion in a process parameter is also in a pixel slightly actually, and the threshold voltage of TFT11b for a drive may become low from the threshold voltage of TFT11a for conversion.
[0182]At this time, since the weak current of subthreshold level flows into TFT11b for a drive also with the signal level below a cutoff level, EL element 15 fine-emits light and the contrast drop of a screen appears. Then, gate length of TFT11b for a drive is made longer than the gate length of TFT11a for conversion. Thereby, even if it changes the process parameter of a thin film transistor within a pixel, the threshold voltage of TFT11b for a drive does not become lower than the threshold voltage of TFT11a for conversion.

[0183]In gate length L, in the comparatively short short-channel-effect field A, the threshold Vth of TFT rises with the increase in gate length L. On the other hand, gate length L is not concerned with gate length L in the comparatively big suppression region B, but the threshold Vth of TFT is almost constant. Gate length of TFT11b for a drive is made longer than the gate length of TFT11a for conversion using this characteristic. For example, when the gate length of TFT11a for conversion is 7 micrometers, the gate length of TFT11b for a drive shall be about 10 micrometers.
[0184]While the gate length of TFT11a for conversion belongs to the short-channel-effect field A, the gate length of TFT11b for a drive may be made to belong to the suppression region B. Thereby, while being able to inhibit the short channel effect in TFT11b for a drive, control of the threshold voltage reduction by change of a process parameter is enabled. By the above, the leakage current of the subthreshold level which flows into TFT11b for a drive can be controlled, fine luminescence of EL element 15 can be suppressed, and it can contribute to a contrast improvement.
[0185]The drive method of the pixel circuit shown in drawing 8 is explained briefly. First, at the time of writing, the 1st scanning line scanA and the 2nd scanning line scanB are made into a selective state. By connecting current source CS to data-line data, where both scanning lines are chosen, the signal current Iw according to brightness information flows into TFT11a for conversion. Current source CS is a variable current source controlled according to brightness information. At this time, since it has connected too hastily electrically by TFT11d for switching between the gate drains of TFT11a for conversion (several 3), a formula is materialized, and the TFT11a for conversion operates in a saturation region. Therefore, between the gate sauce, the voltage Vgs given by a formula (several 1) arises.
[0186]Next, the 1st scanning line scanA and the 2nd scanning line scanB are changed into a non selection

state. If it states in detail, TFT11d for switching will be first changed into an off state by making the 2nd scanning line scanB into a low. The voltage Vgs is held by the capacitor 19 by this. Next, since a pixel circuit and data-line data are electrically intercepted by making the 1st scanning line scanA into a high level, and setting to OFF, the writing to another pixel can be performed via data-line data after that. Here, the data which current source CS outputs as a current level of signal current is validated when the 2nd scanning line scanB serves as non selection, but it may be used as arbitrary levels (for example, write data of the following pixel) after that.

[0187]Since common connection of TFT11a for conversion, a gate, and the sauce is carried out [both], and TFT11b for a drive approaches the inside of a small pixel and is formed, If the TFT11b for a drive is operating in the saturation region, the current which flows through TFT11b for a drive will be given by a formula (several 2), and will turn into the driving current Idd which flows into this [15], i.e., an EL element. What is necessary is just to give sufficient power supply potential to Vdd voltage so that a formula may be materialized in addition (several 3) even if it takes into consideration the voltage drop in EL element 15 in order to operate TFT11b for a drive in a saturation region.

[0188]TFT11e and 11 f may be added and a thereby more good current drive can be realized so that it may illustrate to drawing 9 for the purpose of increasing impedance etc. like drawing 6 (b) etc. drawing 6 explains other matters -- it comes out and omits.

[0189]Thus, direct current voltage was impressed to EL display device explained by produced drawing 6, drawing 8, etc., and the continuation drive was carried out by the constant current density of 10mA[/cm]^2. In EL structure, luminescence of the green (luminescence maximum wavelength lambdamax = 460 nm) of 7.0V and 200 cd/cm^2 has been checked. In a blue light part, a color coordinate by luminosity 100 cd/cm^2 in x= 0.129, y= 0.105, and a green emission part. By luminosity 200 cd/cm^2, the color coordinate was acquired [the color coordinate] for the luminescent color of x= 0.649 and y= 0.338 by luminosity 100 cd/cm^2 in x= 0.340, y= 0.625, and a red light part.

[0190](Embodiment 5) The display, display module and information display device using drawing 6, drawing 8, drawing 9, etc., a drive circuit, a drive method for the same, etc. are explained hereafter.

[0191]In a full color organic electroluminescence display panel, improvement in a numerical aperture becomes an important developing theme. It is for the utilization efficiency of light increasing and leading to a rise in luminosity or reinforcement, if a numerical aperture is raised. What is necessary is just to make small area of TFT which interrupts the light from an organic electroluminescence layer, in order to raise a numerical aperture. Low-temperature polycrystal Si-TFT has one 10 to 100 times the performance of this as compared with an amorphous silicon, and moreover, since the serviceability of current is high, it can make size of TFT very small. Therefore, it is preferred to produce a picture element transistor and a circumference drive circuit with low-temperature-polysilicon art in an organic electroluminescence display panel. Of course, although it may form with amorphous silicon art, a pixel numerical aperture will become quite small.

[0192]By forming drive circuits, such as the gate driver 12 or the source driver 14, on the array substrate 49, the resistance which becomes a problem especially with the organic electroluminescence display panel of a current drive can be lowered. That is, the connection resistance of TCP is lost, and also the leading line from an electrode becomes short 2-3 mm compared with the case of TCP connection, and wiring resistance becomes small. There is an advantage whose process for TCP connection is lost that material cost falls.

[0193]The EL display panel or EL display of (Embodiment 6), next this invention is explained. Drawing 10 is an explanatory view centering on the circuit of an EL display. The pixel 16 is arranged or formed in matrix form. The source driver 14 which outputs the current which performs current programming of each pixel to each pixel 16 is connected. The current mirror circuit corresponding to the number of bits of the video signal is formed in the output stage of the source driver 14. For example, if it is 64 gradation, 63 current mirror circuits are formed for every source signal line, and it is constituted by choosing the number of these current mirror circuits so that desired current can be impressed to the source signal line 18. Especially the minimum output current of one current mirror circuit has 50 or less nA of 10 or more nA of good things to carry out to 35 or less nA of 15 or more nA. This is for securing the accuracy of the transistor which constitutes the current mirror circuit in the source driver 14.

[0194]The precharge or the discharging circuit which emits or charges the electric charge of the source signal line 18 compulsorily is built in. Since the voltage (current) output value of this circuit differs [threshold / of EL element 15] in RGB, it is preferred to constitute so that it can set up independently by R, G, and B.

[0195]As mentioned above, it cannot be overemphasized that a pixel configuration, array constitution, panel structure, etc. which have been explained until now are applied to the composition, method, and device which are explained next.
[0196]It is known that there is the big temperature dependence characteristic (temperature dependenccy characteristics) in an organic EL device. In order to adjust the light-emitting-luminance change by these temperature dependenccy characteristics, nonlinear elements, such as a thermo sensitive register to which output current is changed, or posistor, are added to a current mirror circuit, and reference current is created in analog by adjusting change by temperature dependenccy characteristics with said thermo sensitive register. In this case, since it is uniquely determined by the EL material to choose, the microcomputer etc. which carry out soft control are not needed in many cases. That is, with a liquid crystal material, I hear that it may fix to a fixed shift amount etc., and it is. It is important that temperature dependenccy characteristics change with luminescent color materials, and it is the point that it is necessary to perform optimal temperature-dependenccy-characteristics compensation to every luminescent color (R, G, B).
[0197]Although it cannot be overemphasized that the temperature dependenccy characteristics of EL element 15 of R, G, and B have preferred how to twist, it is necessary to carry out the temperature dependenccy characteristics of each EL element into a fixed range. at least -- the temperature-dependenccy-characteristics direction of R, G, and B -- a uniform direction -- or it is made not to change As for change, it is preferred for each color to be Centigrade 10 ** change, and to make it into 6% or less not less than 3% especially 8% or less not less than 2%.
[0198]Or a microcomputer may perform temperature-dependenccy-characteristics compensation. The temperature of an EL display panel is measured with a temperature sensor, and it is made to change with the measured temperature with a microcomputer (not shown) etc. Reference current etc. may be automatically changed by microcomputer control etc. at the time of a change, and it may control to be able to display a specific menu. It may constitute so that it can change by changing using a mouse etc., using the display screen of an EL display as a touch panel, and displaying a menu, and pressing down a specified part.
[0199]In this invention, the source driver 14 is formed with a semiconductor silicon chip, and is connected with the terminal of the source signal line 18 of the array substrate 49 with glass art on chip (COG). Metallic wiring, such as chromium, aluminum, and silver, is used for wiring of signal wires, such as the source signal line 18. This is because wiring of low resistance is obtained with thin wiring width. Since the metallic wiring can carry out simple [of the process] when a pixel is a reflection type, it is the material which constitutes the reflection film of a pixel, and forming simultaneously with a reflection film is preferred.
[0200]This invention is good also as composition which is not limited to COG technology, loaded the above-mentioned source driver 14 etc. into chip one film (COF) art, and was connected with the signal wire of the display panel. The source driver 14 produces power supply IC102 separately, and is good also as 3 chip configurations.
[0201]A TCF tape may be used. The film for TCF tapes can bond a polyimide film and copper (Cu) foil by thermo-compression, without using adhesives. There are the method of in addition to this carrying out cast molding of the polyimide which dissolved on Cu foil in piles, and the method of attaching Cu by plating or vacuum evaporation on the metal membrane formed by sputtering on the polyimide film in the film for TCP tapes. Although these any may be sufficient, the method of using the TCP tape which attaches Cu to a polyimide film without using adhesives is the most preferred. adhesives are not used for a lead pitch of 30 micrometers or less -- Cu sticks and it corresponds with a laminate sheet. Since the method of Cu sticking and forming a Cu layer by plating or vacuum evaporation in the formation method of a laminate sheet not using these adhesives is suitable for slimming down of the Cu layer, it is advantageous to the minuteness making of a lead pitch.
[0202]On the other hand, the gate driver 12 is low-temperature-polysilicon art, and is formed in the same process as TFT of a pixel. This is because an internal structure is easy as compared with the source driver 14 and clock frequency is also low. Therefore, it can form easily also with low-temperature-polysilicon art, and narrow picture frame-ization can be realized. Of course, the gate driver 12 may be formed with a silicon chip, and it may mount on the array substrate 49 using COG technology etc. Switching elements, such as the pixel TFT, a gate driver, etc. may be formed by elevated-temperature polysilicon technology, and may be formed with organic materials (organic TFT).
[0203]The gate driver 12 contains the shift register 22b the shift register 22a of **, and for the gate signal line 17a gate signal lines 17b. Each shift register 22 is controlled by the clock signal (CLKxP, CLKxN) of a

non-inverter and a negative phase, and a start pulse (STx). In addition, it is preferred to add the enabling (ENABL) signal which controls the output of a gate signal line and a non output, and the up-and-down (UPDWM) signal which carries out the up-and-down inversion of the shift direction. It is preferred to provide the output terminal etc. which, in addition to this, check that the start pulse is shifted and outputted to the shift register. The shift timing of a shift register is controlled by the signal from control IC (not shown). The level shift circuit and inspecting circuit which perform the level shift of external data are built in.

[0204]Since the buffer capacity of the shift register 22 is small, the gate signal line 17 cannot be driven directly. Therefore, between the output gates 24 which drive the output and the gate signal line 17 of the shift register 22, at least two or more inverter circuits 23 are formed.

[0205]Are also the same as when forming the source driver 14 directly on the array substrate 49 by the polysilicon technology of low temperature polysilicon etc., Between the gate of analog switches, such as a transfer gate which drives a source signal line, and the shift register 22 of a source driver, two or more inverter circuits 23 are formed. The following matters (the output of a shift register and the output stage (matter about the inverter circuit arranged among output stages, such as an output gate or a transfer gate) which drives a signal wire are matters common to a source driver and a gate driver circuit.) For example, in drawing 10, illustrated as the output of the source driver 14 was directly connected to the source signal line 18, but. Actually, the multi stage inverter circuit 23 is connected to the output of the shift register 22 of a source driver, and gates of the analog switch, such as a transfer gate, are connected to the output of an inverter circuit.

[0206]The inverter circuit 23 comprises a MOS transistor of P channel, and a MOS transistor of N channel. As explained also in advance, the inverter circuit 23 is connected to the outgoing end of the shift register 22 of the gate driver 12 in multistage, and the final output is connected to the output gate 24. The inverter circuit 23 may consist of only P channels. However, it may constitute not as an inverter circuit but as a mere gate circuit in this case.

[0207]The channel width of TFT of P channel which constitutes each inverter circuit 23, or N channel W, Channel length is set to L (in on double-gate **, the width or channel length of a channel who constitutes is added), and the degree of the inverter near the 1 and display side is set to N (eye N stage) for the degree of the inverter near a shift register.

[0208]Multiplex [of the characteristic difference of the inverter circuit 23 connected if there are many connection number of stageses of the inverter circuit 23] (piled up) is carried out, and a difference arises from the shift register 22 in the transfer time to the output gate 24 (time delay dispersion). In the case of being extreme, to for example, that [one / the output gate 24a / in drawing 10 / (output voltage has changed) / that / 1.0microsec backward (it measures after a pulse is outputted from a shift register)]. The state, one [the output gate 24b / 1.5microsec backward (it measures, after a pulse is outputted from a shift register)] (output voltage has changed), arises.

[0209]Therefore, although a direction with more than [little / inverter circuit / 23 / which is produced between the shift register 22 and the output gate 24] is good, the very larger one of gate width W of the channel of TFT which constitutes the output gate 24 is good. Since the gate driving ability of the output stage of the shift register 22 is small, it is impossible to drive the output gate 24 directly in the gate circuits (NAND circuit etc.) which constitute a shift register. Therefore, although it is necessary to carry out multi stage connection of the inverter, For example, if the ratio of the size of W4/L4 (channel length of the channel width / P channel of P channel) of 23 d of inverter circuits of drawing 10 to the size of W3/L3 of the inverter circuit 23c is large, a time delay will become long and the characteristic of an inverter will also enlarge dispersion.

[0210]Time delay dispersion (dotted line) and the relation of a time delay ratio (solid line) are shown in drawing 11. (Wn-1/Ln-1) / (Wn/Ln) shows a horizontal axis. For example, channel length L of 23 d of inverter circuits and the inverter circuit 23c is the same at drawing 10, and if it is 2W3=W4, it is (W3/L3)/(W4/L4) =0.5. In the graph of drawing 11, a time delay ratio sets the time of (Wn-1 / Ln-1) / (Wn/Ln)=0.5 to 1, and is setting time dispersion as well as delay to 1.

[0211]By drawing 11, the connection number of stages of the inverter circuit 23 increases, so that (Wn-1 / Ln-1) / (Wn/Ln) becomes large, and it is shown that time delay dispersion also becomes large. It is shown that the time delay from the inverter circuit 23 to the inverter circuit 23 of the next step becomes long, so that (Wn-1/Ln-1) / (Wn/Ln) becomes small. It turns out that it is advantageous on a design to make a time delay ratio and time delay dispersion into less than two from this graph. Therefore, what is necessary is just to be able to fulfill the conditions of a following formula.

[0212]The W/L ratio (Wp/Lp) of 0.25<=(Wn-1/Ln-1)/(Wn/Ln)<=0.75 and P channel of each inverter circuit

23 and the W/L ratio (Ws/Ls) of N channel need to fill the following relations.
[0213]There is also little dispersion in a time delay and the number of stages n of the inverter circuit 23 formed between output gates (or transfer gate) from the outgoing end of a shift register at 0.4 <=(Ws/Ls)/(Wp/Lp)<=0.8 pan is good, if a following formula is filled.
[0214]The 3 <=n<=8 mobility mu has a technical problem. If mobility mun of N channel transistor is small, the size of TG and an inverter will become large and power consumption etc. will become large. The forming face product of a driver will become large and panel size will also become large. On the other hand, since it will be easy to cause the characteristic degradation of a transistor if mobility mun is large, mobility mun has the following good ranges.
[0215]The slew rate of the clock signal in 50<=mun<=150 and the shift register 22 is made less than 500v/microsec. It is because degradation of N channel transistor is intense when a slew rate is high.
[0216]A NAND circuit may be sufficient although it presupposed at the output of the shift register that the inverter circuit 23 is connected to multistage by drawing 10. It is because an inverter can be constituted also from a NAND circuit. That is, what is necessary is just to consider the connection number of stages of a gate with the connection number of stages of the inverter circuit 23. Relations, such as a W/L ratio explained also in this case until now, are applied. The matter explained using the above drawing 10 and drawing 11 is applied to drawing 55, drawing 56, drawing 58, etc.
[0217]When the switching transistor of a pixel is P channel in drawing 10 etc., as for the output from the inverter of a final stage, ON state voltage Vgl is impressed to the gate signal line 17, and OFF state voltage Vgh is impressed to the gate signal line 17. On the contrary, when the switching transistor of a pixel is N channel, as for the output from the inverter of a final stage, OFF state voltage Vgl is impressed to the gate signal line 17, and ON state voltage Vgh is impressed to the gate signal line 17.
[0218]Although it presupposed that a gate driver is produced simultaneously with the pixel 16 with elevated-temperature polysilicon or low-temperature-polysilicon art in the above example, it is not limited to this. For example, the source driver 14 and the gate driver 12 which were produced with the semiconductor chip may be separately loaded into the display panel 82 so that it may illustrate to drawing 12.
[0219]When using the display panel 82 for information display devices, such as a cellular phone, it is preferred to mount the source driver 14 and the gate driver 12 in one side of a display panel, as shown in drawing 12 (the gestalt which mounts a driver IC in one side still in this way is called three-side free composition (structure).). Conventionally, the gate driver 12 was mounted X neighborhood of the viewing area, and the source driver 14 was mounted Y neighborhood. It is because it is easy to design the center line of the display screen 21 take the lead in a display and mounting of a driver IC also becomes easy. A gate driver circuit may be produced as composition without three sides using elevated-temperature polysilicon or low-temperature-polysilicon art (it is got blocked and at least one side is directly formed in the array substrate 49 by polysilicon technology among the source drivers 14 and the gate drivers 12 of drawing 12).
[0220]With three-side free composition, not only the composition that loaded or formed IC in the array substrate 49 directly but the composition which stuck on one side (or about one side) of the array substrate 49 the films (TCP, TAB art, etc.) which attached the source driver 14, the gate driver 12, etc. is included. That is, IC means all similar to mounting or the composition which is not attached, arrangement, or it in two sides.
[0221]Like drawing 12, if the gate driver 12 is arranged beside the source driver 14, the gate signal line 17 needs to be formed to the display screen 21 along with C neighborhood (references, such as drawing 13).
[0222]The pitch of the gate signal line 17 formed C neighborhood shall be not less than 5 micrometers 12 micrometers or less. It is because a noise will ride on a contiguity gate signal line under the influence of parasitic capacitance in less than 5 micrometers. According to the experiment, the influence of parasitic capacitance occurs notably at 7 micrometers or less, and image noises, such as the shape of a beat, occur violently in a display screen at less than 5 more micrometers. It is difficult for especially generating of a noise to differ by the right and left of a screen, and to reduce image noises, such as the shape of this beat. If 12 micrometers of reduction are exceeded, the frame width D of a display panel becomes large too much, and is not practical.
[0223]In order to reduce the above-mentioned image noise, it can decrease by arranging the Grant pattern (electric conduction pattern set as fixed voltage at a voltage clamp or the potential stable as a whole) in the lower layer or the upper layer of a portion in which the gate signal line 17 was formed. What is necessary is just to arrange the shield plate (shield foil (electric conduction pattern set as fixed voltage at a voltage clamp or the potential stable as a whole)) formed separately on the gate signal line 17.

[0224]Although the gate signal line 17 of C neighborhood of drawing 13 may be formed with an ITO electrode, in order to low-resistance-ize, it is preferred to laminate and form ITO and a metal thin film, or to form them with a metal membrane. When laminating with ITO, a titanium film is formed on ITO and the alloy thin film of aluminum or aluminum, and molybdenum is formed on it. Or a chromium film is formed on ITO. In the case of a metal membrane, it forms with an aluminum thin film and a chrome thin film. The above matter is the same in other examples of this invention.
[0225]In drawing 13 etc., although the gate signal line 17 presupposes that it arranges in one side of a viewing area, they are not limited to this, and they may be arranged to both. For example, the gate signal line 17a may be arranged on the right-hand side of the display screen 21 (formation), and the gate signal line 17b may be arranged on the left-hand side of the display screen 21 (formation). The above matter is the same in other examples.
[0226]In drawing 14, 1 chip making (1 chip driver IC14c) of the source driver 14 and the gate driver 12 is carried out. If 1 chip making is carried out, mounting of the IC chip to the display panel 82 can be managed with one piece. Therefore, implementation cost can also be reduced. The various voltage used within 1 chip driver IC14c can also be generated simultaneously.
[0227]It is not what is limited to this although the source driver 14, the gate driver 12, and 1 chip driver IC14c are produced with semiconductor wafers, such as silicon, and being mounted in the display panel 82, It may form in the display panel 82 directly by low-temperature-polysilicon art and elevated-temperature polysilicon technology.
[0228]drawing 15 -- the both ends of the source driver 14 -- the gate drivers 12a and 12b -- mounting (or it forms) -- although carried out, it is not limited to this. For example, as shown in drawing 12, while adjoined the source driver 14 and the one gate driver 12 may be arranged to a side. The part illustrated as the thick solid line in drawing 15 etc. shows the part which the gate signal line 17 arranged in parallel and formed. Therefore, the gate signal line 17 for the number of a scanning signal line arranges in parallel the portion (bottom of screen) of b, it is formed, and, as for the portion (upper part of a screen) of a, the one gate signal line 17 is formed.
[0229]Like drawing 15, if the two gate drivers 12a and 12b are used, the number of the gate signal line 17a which is arranged in parallel C neighborhood of drawing 15, and is formed will be set to one half of the number of scanning lines (it is because the number of gate signal lines can be arranged every [2 / 1/] to the right and left of a screen). Therefore, a frame comes to have the feature of becoming equivalent by the right and left of a screen.
[0230]This invention has the feature also in the scanning direction of the gate signal line 17, and a screen separation. For example, the gate driver 12a is connected with the gate signal line 17b of the upper part of a screen in drawing 15. The gate driver 12b is connected with the gate signal line 17a of the bottom of screen. As the arrow A also shows the scanning direction of the gate signal line 17, it is the direction of the upper part of a screen to the lower part. The source signal line 18 is common to the upper part of a screen, and a bottom of screen.
[0231]In drawing 16, it is connected so that the gate driver 12a may differ from the gate signal line 17 with which the upper part of a screen adjoined. The gate driver 12a is connected with the odd-numbered gate signal line 17b. The gate driver 12b is connected with the even-numbered gate signal line 17a. The gate signal line 17b of the scanning direction of a gate signal line is the direction of the upper part of a screen to the lower part (arrow A). The gate signal line 17a is the direction of a bottom of screen to the upper part (arrow B). Thus, by connecting the gate signal line 17 with the gate driver 12, by making the scan method of a gate signal line into a predetermined direction, a luminosity inclination does not occur in the display screen 21, but generating of a flicker can also be controlled again. The source signal line 18 is common to the upper part of a screen, and a bottom of screen. However, it cannot be overemphasized that it may divide by the upper and lower sides of a screen. The above matter is applied to other examples.
[0232]The gate driver 12a is connected with the gate signal line 17b of the upper part of a screen also drawing 14 which is carrying out 1 chip making. The gate driver 12b is connected with the gate signal line 17a of the bottom of screen. The scanning direction of the gate signal line 17b is the direction of the upper part of a screen to the lower part, as the arrow A shows. The scanning direction of the gate signal line 17a is the direction of the lower part of a screen to the upper part, as the arrow B shows. The source signal line 18 is common to the upper part of a screen, and a bottom of screen. Thus, by connecting the gate signal line 17 with the gate driver 12, by making the scan method of a gate signal line into a predetermined direction, a luminosity inclination does not occur in the display screen 21, but generating of a flicker can also be controlled again.
[0233]1 chip driver IC14c is produced with semiconductor wafers, such as silicon, although it presupposes

that it mounts in the display panel 82, it is not limited to this, and it may be directly formed in the display panel 82 by low-temperature-polysilicon art and elevated-temperature polysilicon technology. The driver IC which drives the upper part of a screen may be arranged to the top chord of a display screen, and the driver IC which drives the lower part of a screen may be arranged to the lower side of a display screen (getting it blocked, mounting IC serves as two chips). The above matter is applied also to the example of other this inventions.

[0234]In drawing 14 and drawing 15, it expressed so that a screen might be divided in the center section, but it is not limited to this. For example, in the case of drawing 15, the display screen 21a may be made small, and it may enlarge the display screen 21b. This display screen 21a is made into a partialness viewing area (refer to drawing 17), a time stamp and a date display are mainly performed, and it is used in low-power-consumption mode. In drawing 14 and drawing 15, the display screen 21a is displayed with the gate signal line 17b, and the display screen 21b is displayed with the gate signal line 17a.

[0235]In drawing 17, it is good also as composition which considers the display screen 21a as composition without three sides, and arranges the conventional source driver 14 and the gate driver 12 for the display screen 21b the separate neighborhood so that it may illustrate by drawing 18. That is, I hear that the gate signal line 17a and the source signal line 18a are outputted from 1 chip driver IC14c, and there are.

[0236]The display screen 21 may be divided into two screens, 21a and 21b, and the source driver 14 corresponding to each screen and the gate driver 12 may be arranged so that it may illustrate to drawing 19. Since the writing time of the video signal outputted from each source driver 14 in drawing 19 doubles as compared with other examples, a signal can fully be written in a pixel. The display screen 21 may be set to one and may arrange the source driver 14 to every one upper and lower sides each of a screen so that it may illustrate to drawing 20. This is applicable similarly to the gate driver 12.

[0237]Although it was the composition of the above example having formed the gate signal line 17 in parallel, and wiring to a picture element region, it cannot be overemphasized that the source signal line 18 may be constituted so that it may wire in parallel with one side so that it may not be limited to this and may illustrate to drawing 21.

[0238]In drawing 17, drawing 18, drawing 19, etc., it is also a means effective in low power consumption to change a frame rate (drive frequency or number of times of screen rewriting per unit time (for 1 second)) by the display screens 21a and 21b. It is also effective in low power consumption to change display color numbers or a foreground color by the display screens 21a and 21b.

[0239]The cathode of EL element 15 is connected to Vs1 potential in the composition illustrated by drawing 6. However, there is a problem that the driver voltages of the organic electroluminescence which constitutes each color differ. For example, when the current per [0.01A] unit square centimeter is sent, in blue (B), the terminal voltage of an EL element is 5V, but in green (G) and red (R), it is 9V. That is, terminal voltage differs by B, G, and R. Therefore, in B, G, and R, TFT11c and the sauce drain voltage (SD voltage) of 11 d to hold will differ from each other, and the OFF leakage current between the sauce drain voltage (SD voltage) of a transistor will also differ in each color. If OFF leakage current occurs and OFF leakage characteristics differ in each color, it will be in the complicated displaying condition which a flicker generates after color balance has shifted that correlate with the luminescent color and the gamma characteristic shifts.

[0240]In order to cope with this technical problem, it constitutes from this invention so that it may illustrate to drawing 25, and the potential of one cathode terminal may be changed with the potential of the cathode terminal of other colors among R, G, and B color at least. By drawing 25, B is used as the cathode terminal 53a, and, specifically, G and R are used as the cathode terminal 53b. Although drawing 25 assumes lower extraction which takes out light from a glass surface, there is also a case of upper extraction. In this case, a cathode and an anode become the reversed composition.

[0241]It cannot be overemphasized that it is preferred to make it in agreement as much as possible as for the terminal voltage of EL element 15 of R, G, and B. At least, white peak luminosity is displayed, and in the or more 6000K9000K or less range, as for the terminal voltage of the EL element of R, G, and B, a color temperature needs to carry out material or structure selection so that it may become less than 10V. Less than 2.5V needs to make still more preferably the difference of the greatest terminal voltage of each EL element, and the minimum terminal voltage less than 1.5V among R, G, and B. In the above example, although the color was set to RGB, it is not limited to this. This is explained later.

[0242]Amendment of an irregular color is also required. This irregular color is generated with dispersion in thickness, and dispersion of the characteristic in order to distinguish the EL material of each color by different color with. performing a white raster display by 30% - 70% of luminosity, in order to amend this -- the field of each color in the display screen 21 -- internal division -- cloth is measured. The distribution

within a field is measured one point respectively to at least 30 pixels. This measurement data is saved on the table which consists of memories, and this saved data is used, and it constitutes so that inputted image data may be amended and it may display on the display screen 21.

[0243]Although a pixel is made into the three primary colors of R, G, and B, it may not be limited to this, and three colors of cyanogen, yellow, and magenta may be sufficient as it. Two colors of B and yellow may be sufficient and, of course, monochrome may be sufficient. Six colors of R, G, B, cyanogen, yellow, and magenta may be sufficient, and five colors of R, G, B, cyanogen, and magenta may be sufficient. A color reproduction range expands these as a natural color, and they can realize a good display. In addition, four colors of R, G, B, and white may be sufficient, and eight colors of R, G, B, cyanogen, yellow, magenta, black, and white may be sufficient. The pixel of white light is formed in the display screen 21 whole (production), it may be considered as a three-primary-colors display with light filters, such as RGB, and the luminescent material of each color may be laminated and formed in an EL layer. 1 pixel may be distinguished by different color with like B and yellow. The EL display of this invention is not limited to what performs a colored presentation by the three primary colors of RGB as mentioned above.

[0244]The pixel 16W of white light other than the three primary colors may be formed so that it may illustrate to drawing 22. The pixel 16W of white light is produced by laminating the structure of R, G, and B luminescence (formation or composition), and 1 set of pixels consist of the three primary colors of these RGB, and the pixels 16W of white light. Thus, by forming the pixel of white light, it becomes easy to express white peak luminance, and image display with a feeling of brightness can be realized now.

[0245]Even if it is a case where the three primary colors of RGB are made into 1 set of pixels, it is preferred to change the area of the picture element electrode of each color so that it may illustrate to drawing 23. Of course, balance of the luminous efficiency of each color may be good, and an identical area may be sufficient as long as balance also avoids color purity. However, when the balance of one or more colors is bad, it is preferred to adjust a picture element electrode (emission area), and it should just determine the electrode area of each color on the basis of current density. That is, what is necessary is just to make it the difference of the current density of each color be less than **15% still more preferably less than **30%, when a color temperature adjusts a white balance in the 9000K or less range more than 6000K (kelvin). if current density considers it as 100A / square meter -- the three primary colors -- each -- 70A / square -- more than meter -- 130A / square -- below meter -- further -- desirable -- 85A / square -- more than meter -- 115A / square -- it is made for below meter to become

[0246]It is preferred to arrange by the pixel row which adjoined so that trichromatic arrangement may be differed so that it may illustrate to drawing 24. For example, from the left, if the eventh line is arrangement of R, G, and B, it will consider the oddth line as arrangement of B, G, and R. By arranging in this way, the resolution of the oblique direction of a picture is improved also with a small pixel number. The 1st line may be considered as arrangement of R, G, B, R, G, and B from the left, the 2nd line may be considered as arrangement of G, B, R, G, B, and R, and pixel arrangement may be changed by three or more pixel rows so that the 3rd line may be considered as arrangement of B, R, G, B, R, and G.

[0247]The cathode terminal 53a is formed using the metal mask art which distinguished the organic electroluminescence of each color by different color with. A metal mask is used because organic electroluminescence cannot perform etching etc. in water weakly. Using a metal mask (not shown), the cathode terminal 53a is vapor-deposited and it connects with the contact hole 52a simultaneously. And the B cathode wiring 51a and an electrical link can be taken by the contact hole 52a.

[0248]The cathode terminal 53b is similarly formed using the metal mask art which distinguished the organic electroluminescence of each color by different color with. Using a metal mask (not shown), the cathode terminal 53b is vapor-deposited and it connects with the contact hole 52b simultaneously. The RG cathode wiring 51b and an electrical link can be taken by the contact hole 52b. The aluminum film thickness of a cathode terminal is good to form so that it may be set to not less than 70 nm 200 nm or less.

[0249]Since different voltage can be impressed to the cathode terminals 53a and 53b by the above composition, even if the Vdd voltage of drawing 6 is common to each color, the voltage impressed to the EL element of at least 1 color among RGB can be changed. In drawing 25, although RG considers it as the same cathode terminal 53b, it is not limited to this, and it may be constituted so that it may become a cathode terminal which differs by R and G.

[0250]By constituting as mentioned above, the OFF leakage current between the sauce drain voltage (SD voltage) of a transistor can occur in each color, and a kink phenomenon can be prevented. Therefore, a flicker does not occur, it does not correlate with the luminescent color, the gamma characteristic does not necessarily shift, and good image display can be realized.

[0251]Vs1 of drawing 6 is made into cathode voltage, although it presupposes that this cathode voltage is made to differ in each color, it is not limited to this, and the anode voltage Vdd may be constituted so that it may differ in each color. For example, it is good also as composition which sets Vdd voltage of R pixel to 8V, sets G to 6V and sets B to 10V. As for such anode voltage and cathode voltage, it is preferred to be constituted so that it can adjust in **1V.
[0252]Even if panel size is about 2 inches, about 100-mA current is outputted from the anode connected with Vdd voltage. Therefore, low-resistance-izing of the anode wiring (current supply source line) 20 is indispensable. In order to cope with this technical problem, by this invention, the anode wiring 63 is supplied from viewing-area the upper part and the bottom so that it may illustrate by drawing 26 (both-ends electric supply). By carrying out both-ends electric supply as mentioned above, generating of the luminosity inclination by the upper and lower sides of a screen is lost.
[0253]In order to raise light emitting luminance, it is good to carry out surface roughening of the picture element electrode 48. This composition is shown in drawing 5. First, the La Stampa art is used for the part which forms the picture element electrode 48, and detailed unevenness is formed in it. When a pixel is a reflection type, the metal thin film of about 200-nm aluminum is formed by sputtering process, and the picture element electrode 48 is formed. Surface roughening of the heights is provided and carried out to the part where the picture element electrode 48 touches an organic EL device. In the case of a simple matrix type display panel, the picture element electrode 48 makes it a stripe like electrode. Heights may not be limited only to convex and a concave may be sufficient as them. Concave and a convex may be formed simultaneously.
[0254]The size of a projection the average value of about 4 micrometers in diameter, and the distance between contiguity 10 micrometers, 20 micrometers, It turned out that 40 micrometers is used, and light emitting luminance becomes strong about the unit area density of a projection, respectively, so that the unit area density of a projection becomes large when the measurement of luminance is performed as 1000-1200-piece [/mm] ^{2}, 100-120-piece [/mm] ^{2}, and 600-800-piece [/mm] ^{2}. Therefore, it turned out that the surface state of a picture element electrode is changed and light emitting luminance can be adjusted by changing the unit area density of the projection on the picture element electrode 48. According to examination, the good result was able to be obtained because below 800-piece [/mm] ^{2} carries out [more than 100 piece //mm / ^{2}] unit area density of a projection.
[0255]Organic electroluminescence is a self-light emitting device. If the light by this luminescence enters into TFT as a switching element, a phot conductor phenomena (contest the phot) will occur. In contest a phot, the phenomenon whose leak (off-leak) in the time of OFF of switching elements, such as TFT, increases by optical pumping is said.
[0256]In order to cope with this technical problem, as shown in drawing 27, the light-shielding film 91 is formed in the lower layer of the gate driver 12 (depending on the case, it is the source driver 14), and the lower layer of pixel TFT11 by this invention. The light-shielding film 91 is formed with metal thin films, such as chromium, and sets the thickness to not less than 50 nm 150 nm or less. It is because shielding effects are scarce when thickness is thin, unevenness will occur and patterning of TFT11 of the upper layer will become difficult, if thick.
[0257]The smoothing film 71a which consists of not less than 20-nm an inorganic material of 100 nm or less is formed on the light-shielding film 91. Or one electrode of the capacitor 19 may be formed using the layer of this light-shielding film 91. In this case, it is preferred to make the smoothing film 71a thinly as much as possible, and to enlarge capacity value of a capacitor. The light-shielding film 91 may be formed with aluminum, a silicon oxide film may be formed in the surface of the light-shielding film 91 using anodization art, and this silicon oxide film may be used as a dielectric film of the capacitor 19. On the smoothing film 71b, the picture element electrode of a high aperture (HA) structure is formed.
[0258]The gate driver 12 should control not only a rear face but penetration of the light from the surface. It is because it malfunctions under the influence of contest a phot. Therefore, in this invention, when a cathode terminal is a metal membrane, a cathode terminal is formed also in the surfaces, such as the gate driver 12, and this electrode is used as a light-shielding film.
[0259]However, if a cathode terminal is formed on the gate driver 12, malfunction of the driver by the electric field from this cathode terminal or the electric interengagement of a cathode terminal and a driver circuit may occur. In order to cope with this technical problem, in this invention, at least one layer of organic electroluminescence films of two or more layers are preferably formed simultaneously with the organic electroluminescence film formation on a picture element electrode on the gate driver 12 etc. Fundamentally, since an organic electroluminescence film is an insulating material, by forming an organic

electroluminescence film on a gate driver, between a cathode and a gate driver is isolated and it can cancel the above-mentioned technical problem.

[0260]In a pixel, if between the terminals of one or more TFT11, or TFT11 and a signal wire short-circuit, EL element 15 may always light up and may serve as a luminescent spot. Since this luminescent spot is visually conspicuous, it is necessary to sunspot-ize it (astigmatism light). As these ways of coping, the applicable pixel 16 is detected, the capacitor 19 is irradiated with a laser beam, and between the terminals of a capacitor is short-circuited. Since it becomes impossible to hold an electric charge to the capacitor 19, TFT11 stops then, sending current.

[0261]In this case, it is desirable to remove the cathode film which corresponds to the position which irradiates with a laser beam. This is to prevent the terminal electrode and cathode film of the capacitor 19 from short-circuiting by laser beam exposure.

[0262]The structure illustrated to drawing 28 is also illustrated. Drawing 28 is an example of the lower extraction structure which takes out light from the array substrate 49 side. The light-shielding film is formed in the lower layer of the gate driver 12 (depending on the case, it is the source driver 14), and the lower layer of pixel TFT11 also in drawing 28.

[0263]However, since it malfunctions under the influence of contest a phot, the gate driver 12 (or source driver 14) should control not only a rear face but penetration of the light from the surface. For this reason, in this invention, the cathode terminal 46 is used as a light-shielding film.

[0264]When a cathode (or anode) electrode is a transparent electrode, on the other hand, a jam, When it is the structure (as for taking out light from the array substrate 49 side, it is upper extraction to take out light from lower drawing and EL film vacuum evaporation side) of Mitsukami extraction which considers a picture element electrode as a reflective type, and uses a common electrode as transparent electrodes (ITO, IZO, etc.), the sheet resistance values of a transparent electrode pose a problem. Although a transparent electrode is high resistance, it is because it is necessary to send current through the cathode of organic electroluminescence with high current density. Therefore, if a cathode terminal is formed by the monolayer of an ITO film, it will be in a heated state by generation of heat, or the luminosity inclination of a degree occurs very much in a display screen.

[0265]In order to cope with this technical problem, the low resistance-ized wiring 92 which consists of a metal thin film on the surface of a cathode terminal is formed. The low resistance-ized wiring 92 is the same composition (it is thickness (50 nm - 200 nm) at chromium or the charge of an aluminum material) as the black matrix (BM) of a liquid crystal display panel, and it is the same position (between picture element electrodes, on the gate driver 12, etc.). However, in organic electroluminescence, since it is not necessary to form BM, functions completely differ. The low resistance-ized wiring 92 is not limited to the surface of the transparent electrode 72, and may be formed in a rear face (field which touches an organic electroluminescence film). Aluminum and magnesium, such as an alloy or laminated structure bodies, such as Mg-Ag, Mg-Li, and aluminum-Li, indium, copper, or each alloy may be used as a metal membrane formed in the shape of BM. In order to prevent corrosion etc. on BM, ITO and an IZO film are laminated further and organic thin films, such as inorganic thin films, such as SiNx and SiO_2, or polyimide, are formed.

[0266]When taking out light from the vacuum evaporation side of EL film (upper extraction), it is preferred to form Mg-Al film on the organic electroluminescence layer 47, and to form ITO and an IZO film on it. Or it is preferred to form Mg-Al film on the organic electroluminescence layer 47, and to form a black matrix (a black matrix like a liquid crystal display panel) on it. As for this black matrix, it is preferred to form by chromium, aluminum, Ag, Au, Cu, etc., and to form on this the protective film 1761 which consists of organic compound insulators, such as inorganic insulating films, such as SiO_2 and SiNx, polyester, an acrylic. It is preferred to form an antireflection film (AIR coat) on this protective film 1761. The minimum thickness of the protective film 1761 shall be 1 micrometers or more.

[0267]Even if it is a case of lower extraction, there is an effect also in making high transmissivity of the reflection film 46 of a cathode terminal. Even if this is the composition of seeing a display image from the array substrate 49 side, since the transmissivity of the reflection film 46 is high, a reflect lump decreases and it becomes unnecessary [the circular light board 74]. Therefore, optical extraction efficiency may improve rather than upper extraction. As for especially the transmissivity of the reflection film 46, it is preferred to make it to 90% or less not less than 70% not less than 60% of 90% or less. While the sheet resistance values of a cathode terminal become it low that it is 60% or less, it is because a reflect lump becomes large. On the contrary, it is because the sheet resistance values of a cathode terminal become high and the luminosity inclination of a display image becomes large at not less than 90%.

[0268]For making transmissivity of the reflection film 46 high, an Al film is thinly formed like not less than

20-nm100 nm or less in thickness. It is preferred to form ITO and an IZO film on it. Or it is preferred to form a black matrix on an Al film.
[0269]The emission area of the organic electroluminescence layer 47 becomes large by making the picture element electrode 48 circular so that it may illustrate to drawing 29. Therefore, current density becomes small and high lifetime-ization of EL element 15 can be realized. Since the terminal voltage of EL element 15 also falls, power efficiency also improves.
[0270]Drawing 30 is an explanatory view of the manufacturing method of the EL display panel explained by drawing 29. TFT11, the gate driver 12, etc. are formed on the array substrate 49 so that it may illustrate by drawing 30 (a).
[0271]Next, the smoothing film 71 which consists of organic materials, such as an acrylic resin, is applied on the array substrate 49 so that it may illustrate to drawing 30 (b). The smoothing films 71 may be inorganic materials, such as SOG. As for thickness, it is preferred to use not less than 1.5 micrometers 3 micrometers or less. Next, the mask 1771 is formed on said smoothing film 71. The mask 1771 is formed with a metallic material and it is made for a formation position to correspond to the pixel 16. Next, it etches. Any of dry etching, such as wet etching and O_2 plasma, may be sufficient as etching. Since the smoothing film 71 is etched, the smoothing film 71 becomes circular from between the masks 1771 so that it may illustrate to drawing 30 (c).
[0272]A mask (not shown) is formed in the smoothing film 71, and the contact hole 1772 is formed so that it may illustrate to drawing 30 (d). Or the contact hole 1772 is also simultaneously formed by the etching process of drawing 30 (b).
[0273]Next, the picture element electrode 48 is formed with transparent electrodes, such as ITO and IZO, so that it may illustrate to drawing 30 (e). The picture element electrode 48 and TFT11 take connection by the pixel contact part 1751. The picture element electrode 48 and drain terminal which consist of ITO(s) in this contact hole are electrically connected.
[0274]Next, not less than 50-nm a carbon film of 150 nm or less is thinly vapor-deposited on the picture element electrode 48, and an organic electroluminescence layer is formed on this. In a monochromatic case, in the case of RGB, the organic electroluminescence layer 47 uses a metal mask for the whole surface, and is distinguished by different color with on it (refer to drawing 30 (f)).
[0275]Al film (reflection film) 46 used as a cathode terminal is formed after formation of the organic electroluminescence layer 47 (drawing 30 (g)). The protective film 1761 is formed on Al film (reflection film) 46 (drawing 30 (h)).
[0276]The protective film 1761 may be the protective layer which used the film. For example, using for the film of an electrolytic condenser what vapor-deposited DLC (diamond- -like carbon) as a protective layer is illustrated. Moisture perviousness is very bad (moisture proof) one, and can use this film as the protective layer 1761. The thickness of the protective layer 1761 is n-d (n synthesizes and (n-d of each thin film is calculated) calculates those refractive indicees, when the refractive index of a thin film and two or more thin films are laminated.). d synthesizes and calculates those refractive indicees, when the thickness of a thin film and two or more thin films are laminated. It is good to make it below the luminescence dominant wavelength lambda of EL element 15 become.
[0277]The organic electroluminescence layer 47 or the picture element electrode 48 may not be limited circularly, and triangular pyramid shape, conical shape, and the shape of a sine curve may have as it, and the structure which combined these may be sufficient as it. It may be the composition that triangular pyramid shape, conical shape, and the shape of a sine curve should have been formed, these had combined enough on the circle detailed to 1 pixel, or random unevenness was formed. Although convex is circular and it is in drawing 29, even if a concave is circular, it is the same as that of the above.
[0278]Drawing 31 is the panel-ized lineblock diagram (sectional view). although other drawings are the same, in order that each drawing may draw an understanding easily in this specification -- an abbreviation -- scaling is carried out. Also in the sectional view of the display panel of drawing 31, the smoothing film 71 etc. are illustrated thickly enough. However, the board thickness of the array substrate 49 is illustrated very thinly. TFT is omitting.
[0279]In drawing 31, the spacer 1781 is arranged between the closure lid 41 and the array substrate 49, and directly, the protective film 1761, the reflection film 46, or the organic electroluminescence layer 47 and the closure lid 41 is constituted so that it may not touch. The periphery of the viewing area is arranged or filled up with the drier. A thing cylindrical [a spacer] or spherical is used. As for height, it is preferred to use not less than 10 micrometers 100 micrometers or less. It can also be considered as a spacer by processing the protective film 1761. That is, the function of a spacer is given for a part or all of the protective film 1761 protuberance form or by pillar-shaped, processing it or forming in stripe shape. The

composition which uses the spacer 1781 as a drier is also preferred.
[0280]As for the pixel shown in drawing 8, TFT11b for a drive and TFT11a for conversion have a relation of a current mirror, and its characteristics (the threshold Vt, S value, mobility mu, etc.) of these must correspond. In the pixel of drawing 6, it cannot be overemphasized that it is preferred that the characteristic of each TFT is in agreement.
[0281]As for the semiconductor membrane which constitutes TFT11 of the pixel 16, in low-temperature-polysilicon art, forming by laser annealing is common. Dispersion in the conditions of this laser annealing turns into dispersion in the TFT11 characteristic. However, in the method which performs current programming, such as drawing 6 and drawing 8, if the characteristic of TFT11 in 1-pixel 16 is in agreement, it can drive so that predetermined current may flow into EL element 15. This point is an advantage which is not in a voltage program.
[0282]To this technical problem, by this invention, as shown in drawing 32, it irradiates with the laser radiation spot 230 at the time of annealing in parallel with the source signal line 18. The laser radiation spot 230 is moved so that it may be in agreement with one pixel row. Of course, for example, it may irradiate with laser not in the thing limited to one pixel row but in the unit [RGB / 1 pixel] of drawing 32 16 (in this case, it will be called three pixel rows). Especially the pixel is produced so that it may become square shape at 3 pixels of RGB. Therefore, each pixel of R, G, and B serves as longwise picture element shape. Therefore, arrangement of TFT11 formed in the pixel 16 is arranged in a lengthwise direction so that it may illustrate to drawing 32 (TFT11a for conversion, TFT11b for a drive). Therefore, characteristic dispersion of TFT11 can be prevented from generating within 1 pixel by making the laser radiation spot 230 longwise and annealing it.
[0283]Generally, the length of the laser radiation spot 230 is a fixed value like 10 inches. Since this laser radiation spot 230 is moved, it is necessary to arrange a panel so that it may be stored within limits which can move the one laser radiation spot 230 (it is got blocked and the laser radiation spot 230 is kept from lapping in the center section of the display screen 21 of a panel).
[0284]In the composition of drawing 33, it is formed so that three panels may be perpendicularly arranged within the limits of the length of the laser radiation spot 230. The annealer which irradiates with the laser radiation spot 230 recognizes the positioning markers 242a and 242b of the glass substrate 241, and moves the laser radiation spot 230. A pattern recognition device performs recognition of the positioning marker 242. An annealer (not shown) recognizes the positioning marker 242 and deduces the position of a pixel row. And it irradiates with the laser radiation spot 230, and annealing is performed one by one so that it may lap with a pixel row position exactly.
[0285]As for especially the laser annealing method (method which irradiates with the laser spot of line form in parallel with the source signal line 18) explained by drawing 32 and drawing 33, it is preferred to adopt at the time of the current programming method of an organic EL panel. Because, it is because the parallel direction of a source signal line and the characteristic of TFT11 are in agreement (the characteristic of the pixel TFT which adjoined the lengthwise direction approximates). Therefore, there is little change of the voltage level of a source signal line at the time of a current drive, and it is hard to generate current writing shortage (for example, since the current which is sent through TFT11a for conversion of each pixel which adjoined in the case of a white raster display is almost the same, there is little change of the current amplitude outputted from the source driver 14).
[0286]By the method which carries out the simultaneous writing of two or more pixel rows explained by drawing 34, drawing 35, etc., uniform image display is realizable (it is because it is hard to generate the display unevenness which originates mainly in dispersion in a TFT characteristic). Since drawing 34 chooses two or more pixel line simultaneously, if TFT of the pixel which adjoined is uniform, the TFT characteristic unevenness of a lengthwise direction can be absorbed with the source driver 14.
[0287]As shown in drawing 6, the gate signal line 17a will be in switch-on (since TFT11 of drawing 6 is P channel transistor here, it is flowed with a low level) at a line selection period, and the gate signal line 17b will be in switch-on at the time of a non selection period.
[0288]If the parasitic capacitance of the source signal line 18 increases as it is shown in the solid line a of drawing 36, when the state of a source signal line is gradation 0 displaying condition, the current value over the gradation 1 is impressed and a line selection period is operated in 75 microseconds, the current value outputted to EL element 15 will decrease.
[0289]The dotted line b of drawing 36 is a case where the current value over the gradation 1 is passed 10 times compared with the solid line a, and the decrease proportion of the current value outputted to EL element 15 becomes small to the increase in the parasitic capacitance of the source signal line 18. Since about 10% of dispersion cannot be observed as a difference of luminosity for human being's eyes to a fixed

current value, the sauce capacity permitted supposing it accepts about 10% of fall is set to 25 pF or less with 2 pF or less and the dotted line b as the solid line a.
[0290]The time t which current value change of the source signal line 18 takes. If the current which flows the size of stray capacitance through the voltage of C and a source signal line into V and a source signal line is set to I, Since it is t=C-V/I, that a current value can be enlarged 10 times can do short time which current value change takes to about 1/10, or even if sauce capacity increases 10 times, it is shown that it can change to a predetermined current value. Therefore, in order to write in a predetermined current value within a short horizontal scanning period, it is effective to make a current value increase.
[0291]In order to obtain predetermined luminosity so that output current will also be 10 times and the luminosity of an EL element may be 10 times if an input current is increased 10 times, the "on" period of TFT11d for switching of drawing 6 is made into 1/10 [conventional], and predetermined luminosity was displayed by making a light emission period into 1/10. That is, in order to fully perform the charge and discharge of the parasitic capacitance of the source signal line 18 and to program a predetermined current value to TFT11a for conversion of the pixel 16, it is necessary to output comparatively big current from the source driver 14. However, if big current in this way is sent through the source signal line 18, this current value will be programmed by the pixel, and big current flows into EL element 15 to predetermined current. For example, if it programs with 10 times as much current, naturally 10 times as much current will flow into EL element 15, and EL element 15 will emit light by one 10 times the luminosity of this. That is, what is necessary is just to make time to flow into EL element 15 into 1/10, in order to use predetermined light emitting luminance. By driving in this way, the charge and discharge of the parasitic capacitance of the source signal line 18 can fully be carried out, and predetermined light emitting luminance can be obtained.
[0292]This is an example, although one 10 times the current value of this is written in TFT11a for conversion of a pixel (the terminal voltage of the capacitor 19 is set up correctly) and ON time of EL element 15 is made into 1/10. Depending on the case, one 10 times the current value of this is written in TFT11a for conversion of a pixel, and it is good as for 1/5 in the ON time of EL element 15. On the contrary, one 10 times the current value of this may be written in TFT11a for conversion of a pixel, and the ON time of EL element 15 may be doubled. This invention making the write current to a pixel values other than a predetermined value, making into an intermittent condition the current which flows into EL element 15, and driving has the feature. In this specification, in order to explain easily, one N times the current value of this is written in TFT11 of a pixel, and it explains increasing the ON time of EL element 15 1/N time. However, not the thing limited to this but an N1 time current value is written in TFT11 of a pixel, and it cannot be overemphasized that it is good also considering the ON time of EL element 15 as 1/N twice (it differs in N1 and N2). The interval which carries out an intermission is not limited at equal intervals.
[0293]In order to explain easily, it explains setting these 1F to 1/N on the basis of 1F (1 field or one frame). However, since one pixel row is chosen, and there is time (usually one horizontal scanning period (1H)) when a current value is programmed and an error is also produced depending on a scanning state, the above explanation is only a problem of the shape of facilities for explaining easily to the last, and is not limited to this.
[0294]An organic (inorganic matter) EL display has a technical problem also in the point that the method of presentation differs from the display which displays a picture as a set of a line display with an electron gun like CRT fundamentally. That is, in an EL display, the current (voltage) written in the pixel is held between the periods of 1F (1 field or one frame). Therefore, if the animation is displayed, the technical problem that outline dotage of a display image occurs will be generated.
[0295]In this invention, during the period of one F/N sends current through EL element 15, and other periods (1F(N-1) /N) do not send current. The case where carried out this drive system and one point of a screen is observed is considered. In this displaying condition, an image data display and a black display (astigmatism light) are repeatedly displayed for everyF. That is, an image data displaying condition will be in a discontinuous display (intermittent display) state in time. If a video data display is seen by this intermittent displaying condition, outline dotage of a picture is lost and a good displaying condition can be realized. That is, animation display near CRT is realizable. Although an intermittent display is realized, the main clocks of a circuit are not different from the former. Therefore, the power consumption of a circuit does not increase.
[0296]The image data (voltage) which light modulation is made in the case of a liquid crystal display panel is held at the liquid crystal layer, and if it is going to carry out a black insertion display, it needs to rewrite the data currently impressed to a liquid crystal layer. Therefore, since the operation clock of the source driver 14 must be made high and image data must be impressed to the source signal line 18 a black indicative data and by turns, in order to realize a black insertion display (intermittent display of a black

display etc.), it is necessary to raise the main clocks of a circuit. The image memory for carrying out time-axis extension is also needed.
[0297]However, in the pixel configuration of the EL display panel of this invention. As shown in drawing 6, drawing 56, drawing 61 - drawing 65, drawing 68 - drawing 72, drawing 74, drawing 75, Drawing 127, Drawing 130, Drawing 152, etc., image data is held at the capacitor 19 and is sending the current corresponding to the terminal voltage of this capacitor 19 through EL element 15. Therefore, image data is not held like a liquid crystal display panel at a light modulation layer.
[0298]This invention controls the current sent through EL element 15 only by making TFT11d for switching, or TFT11e turn on and off. That is, even if it turns off the current Iw which flows into EL element 15, image data is held as it is at the capacitor 19. Therefore, if a switching element etc. are made one [the following timing] and current is sent through EL element 15, the flowing current is the same as that of the current value which was flowing before. When it is going to realize a black insertion display (intermittent display of a black display etc.), it is not necessary to raise the main clocks of a circuit with this invention. Since it is not necessary to carry out time-axis extension, an image memory is also unnecessary. Time after impressing current until it emits light is short, and the organic EL device 15 is a high speed response. Therefore, it is suitable for animation display and the problem of the animation display which is a problem of conventional data-hold type display panels (a liquid crystal display panel, an EL panel, etc.) can be solved by carrying out an intermittent display further.
[0299]As shown in drawing 37, as for the gate signal line 17b, an "on" period is 1F (since program time is usually 1H and the number of pixel rows of an EL display is at least 100 or more lines when current programming time is set to 0) conventionally. If sauce capacity is about 20 pF, it can change from the gradation 0 which will start [according to drawing 36] change most as for time if it supposes that an error is 1% or less also as 1F and is referred to as N= 10 also to the gradation 1 in about 75 microseconds. If this is an EL display about 2 type, it shows that frame frequency can drive at 60 Hz.
[0300]What is necessary is just to make source current into 10 or more times, when sauce capacity becomes large with a large-sized display. What is necessary is generally, just to make the "on" period of the gate signal line 17b (TFT11d) into 1 F/N, when a source current value is increased N times. Thereby, it is applicable to television, the display for a monitor, etc.
[0301]Hereafter, it explains in more detail, referring to drawings. First, the parasitic capacitance 404 of drawing 6 is generated with the connection capacity between source signal lines, the buffer output capacity of the source driver 14, the cross capacity of the gate signal line 17 and the source signal line 18, etc. This parasitic capacitance 404 is usually set to not less than 10 pF. Since voltage is impressed to the source signal line 18 by low impedance from the source driver 14 in a voltage drive, the parasitic capacitance 404 does not become large with a problem by drive somewhat.
[0302]However, in a current drive, it is necessary especially to program the capacitor 19 of a pixel according to the micro current of 5 or less nA by the image display of a black level. Therefore, if the parasitic capacitance 404 occurs in the size beyond a predetermined value, the charge and discharge of the parasitic capacitance cannot be carried out within time (since less than [1H], however two pixel rows may usually be written in simultaneously, not limited to less than [1H]) to program to one pixel row. If charge and discharge cannot be carried out in 1H period, it becomes the writing shortage to a pixel and resolution does not come out at all.
[0303]In the case of the pixel configuration of drawing 6, as shown in drawing 7 (a), the program current I1 flows into the source signal line 18 at the time of current programming. This current I1 flows through TFT11a for conversion, and the 19 capacitorV1 is set up so that the current which sends the program current I1 may be held (program). At this time, TFT11d for switching is an open condition (OFF state).
[0304]Next, TFT11 operates like drawing 7 (b) in the period which sends current through EL element 15. That is, OFF state voltage Vgh is impressed to the gate signal line 17a, and TFT11a for conversion and TFT11c for taking in turn off. On the other hand, one [ON state voltage Vgl is impressed to the gate signal line 17b, and / TFT11d for switching].
[0305]Now, supposing the program current I1 is N times the current (predetermined value) originally sent, the current which flows into EL element 15 of drawing 7 (b) will also be set to I1. Therefore, EL element 15 emits light by one N times the luminosity of a predetermined value.
[0306]Then, if only the period of 1/N of time (about 1F) originally is made one and other period (N-1)/N are made to turn off, the average luminance of the 1F whole will turn into predetermined luminosity.
[TFT11d for switching] This displaying condition is approximated with CRT scanning the screen with the electron gun. The range as which a different point displays the picture is the point which 1/N (the full screen is set to 1) of the whole screen has turned on (in CRT, the turned-on range is one pixel row

(strictly 1 pixel)).
[0307]In this invention, as the image display region of this 1/N shows drawing 38 (a1), it moves downward from on the display screen 21. In this invention, current flows into EL element 15 and, as for other periods (1F-(N-1)/N), current does not flow only between 1 F/N periods. Therefore, although a picture serves as an intermittent display, since it will be in the state where the picture was held by the afterimage to human being's eyes, it seems to display the full screen uniformly.
[0308]In this displaying condition, an image data display and a black display (astigmatism light) are repeatedly displayed for everyF. That is, an image data displaying condition will be in a discontinuous display (intermittent display) state in time. In the liquid crystal display panel (EL display panels other than this invention), since data was held during 1F at the pixel, when it was animation display, even if image data changed, the change could not be followed, but it had become animation dotage (outline dotage of a picture). However, in this invention, since the picture is indicated by intermittent, outline dotage of a picture is lost and a good displaying condition can be realized. That is, animation display near CRT is realizable.
[0309]There is also no contrast drop like [at the time of indicating the liquid crystal display panel by intermittent in an EL display, since the black display was completely astigmatism light]. As shown in drawing 7, an intermittent display is realizable only by carrying out on-off operation of the TFT11d for switching. This is because the memory of the image data is carried out to the capacitor 19. That is, image data is held during 1F at each pixel 16. Control of TFT11d for switching has realized whether the current equivalent to this image data currently held is sent through EL element 15.
[0310]Therefore, it is changeless to the number of TFT11 which constitutes 1 pixel from a case where it is not considered as the case where an intermittent display is realized. That is, the pixel configuration remained as it was, removed the influence of the parasitic capacitance 404 of the source signal line 18, and has realized good current programming. Moreover, animation display near CRT is realized.
[0311]As for the operation clock of the gate driver 12, since it is late enough as compared with the operation clock of the source driver 14, the main clocks of a circuit do not necessarily become high. Change of the value of N is also easy.
[0312]An image display direction (the direction of image writing) is made down from on a screen by the 1st field eye (drawing 39 (a)), and is good also as above (drawing 39 (b)) from under a screen by the following 2nd field eye so that it may illustrate to drawing 39. That is, what is necessary is just to repeat drawing 39 (a) and drawing 39 (b) by turns.
[0313]By the 1st field eye, it is considered as down from on a screen so that it may illustrate to drawing 40 (drawing 40 (a)), Once considering the full screen as the black display (non display regions) 312 (drawing 40 (b)), by the following 2nd field eye, it is considered as above (drawing 40 (c)) from under a screen, and is once good also considering the full screen as the black display (non display regions) 312 (drawing 40 (d)). That is, what is necessary is just to repeat the state of drawing 40 (a) to drawing 40 (d) by turns.
[0314]In drawing 39, drawing 40, etc., although how to write in a screen was carried out the bottom or the bottom to the top from on the screen, it is not limited to this. The above matter is the same also in the example of other this inventions.
[0315]Drawing 38 (a) sets the image display region 311 to 1/N, and is setting the non display regions 312 to (N-1) / N (however, this is a case of an ideal state.). Since there are the capacitor 19 and a thrust omission by the sauce gate (SG) capacity of TFT11a for conversion actually, it differs. That is, it is a case where the image display region 311 is set to one. The image display region 311 is moved to down from on a screen, as shown in an arrow (drawing 38 (a1) -> drawing 38 (a2) -> drawing 38 (a3) -> drawing 38 (a1) ->). However, though movement of this image display region 311 is not limited to moving to down from on a screen and moves to above from under a screen, it is good. It cannot be overemphasized that it may scan so that the 1st (1 field eye) frame may be moved to down from on a screen and the following frame [2nd (2 field eye)] may move to above from under a screen (operation). It may scan from the right of a screen from the left or the left of a screen to the right (operation).
[0316]Drawing 37 is an operation timing waveform. As indicated also in advance, it supposes that one screen is displayed in the period of 1F, and it is supposed that current programming will be carried out in the period of 1H. Drawing 37 (a) shows the timing waveform of the gate signal line 17a in drawing 6 (a) and (b). Drawing 37 (b) shows the timing waveform of the gate signal line 17b. Fundamentally, when the gate signal line 17b reaches ON state voltage Vgl, TFT11d for switching flows (a period is 1 F/N), in peak current, N times as much current as the predetermined current I1 flows into EL element 15, and EL element 15 emits light by the luminosity B (N-B) N times the luminosity of predetermined. TFT11d for switching will be in an OFF state during 1F/(N-1)/N. Control of this gate signal line is easily realizable like

drawing 10 by controlling two shift registers (22a, 22b) in the gate driver 12. It is because the shift register 22a holds the control data of the gate signal line 17a (scan) and the shift register 22b should just hold the control data of the gate signal line 17b (scan).
[0317]Drawing 41 shows the waveform of the gate signal line 17b. When drawing 41 (a) is made into the voltage waveform of the gate signal line 17b of the 1st pixel row eye, drawing 41 (b) shows the voltage waveform of the gate signal line 17b of the 2nd pixel row eye which adjoined the 1st pixel row eye. Similarly, drawing 41 (c) shows the voltage waveform of the gate signal line 17b of the following 3rd pixel row eye, and drawing 41 (d) shows the voltage waveform of the gate signal line 17b of the 4th pixel row eye.
[0318]As mentioned above, make the same the waveform of the gate signal line 17b by each pixel row, and it is made to shift at the interval of 1H, and impresses. Since the pixel row turned on one by one can be shifted specifying the time which EL element 15 has turned on by scanning in this way to 1 F/N, it is easy to make the same the waveform of the gate signal line 17b, and to shift it by each pixel row. It is because what is necessary is just to control ST1 and ST2 which are data impressed to the shift registers 22a and 22b of drawing 10. For example, when ON state voltage Vgl is outputted to the gate signal line 17b when input ST2 is L level, and input ST2 is H level, supposing OFF state voltage Vgh is outputted to the gate signal line 17b, Only the period of 1 F/N inputs ST2 impressed to the gate signal line 17b on L level, and other periods are used as H level. This ST2 inputted is only shifted by clock CLK2 in sync with 1H.
[0319]Similarly, creation of the waveform of the gate signal line 17a shown in drawing 37 (a) is also easy. It is because what is necessary is just to control ST1 which is input data of the shift register 22a of drawing 10. For example, when ON state voltage Vgl is outputted to the gate signal line 17a when input ST1 is L level, and input ST1 is H level, supposing OFF state voltage Vgh is outputted to the gate signal line 17a, Only the period of 1H inputs ST1 impressed to the gate signal line 17a on L level, and other periods are used as H level. This ST1 inputted is only shifted by clock CLK1 in sync with 1H.
[0320]It is the example which drawing 38 (b) made the image display region 311 1/(2N), and moved the two image display regions 311a and 311b to down from on the screen as shown in an arrow (drawing 38 (b1) -> drawing 38 (b2) -> drawing 38 (b3) -> drawing 38 (b1) ->). However, though movement of these image display regions 311a and 311b is not limited to moving to down from on a screen and moves to above from under a screen, it is good. It cannot be overemphasized that it may scan so that the 1st (1 field eye) frame may be moved to down from on a screen and the following frame [2nd (2 field eye)] may move to above from under a screen (operation). It may scan from the right of a screen from the left or the left of a screen to the right (operation).
[0321]It is the example which drawing 38 (c) made the image display region 311 1/(3N), and moved the three image display regions 311a, 311b, and 311c to down from on the screen as shown in an arrow (drawing 38 (c1) -> drawing 38 (c2) -> drawing 38 (c3) -> drawing 38 (c1) ->).
[0322]As shown in drawing 38 (b) and (c), the more it divides the image display region 311 into plurality, the more the frame rate (rewrite a screen in the number of times 60 which writes a screen in 1 second, for example, a frame rate, 60 times in 1 second) of the whole image display can be reduced. If a frame rate is reduced, since the operation clock of the part and a circuit can be reduced, power consumption can be made small. That is, since the light emission period of EL element 15 becomes short, and the instant luminosity on appearance becomes high and the image display region 311 and the non display regions 312 are moreover repeated at high speed, a flicker decreases. Therefore, a frame rate can be reduced.
[0323]By making it drive as mentioned above, the number of times turned on in one frame (1 field) can be increased, and a flicker can be reduced. Since a frequency component becomes high by increasing the number of times of lighting in lighting of an EL element, human being's eyes become is hard to be observed. For example, when the lighting period per time is set to one seventh and one frame was switched on 7 times, the display as for which frame frequency does not have a flicker in 30 Hz has been realized.
[0324]The luminosity of a picture can be adjusted by controlling turning on and off of TFT11d for switching (variable). For example, in the case of drawing 38 (a), the luminosity of the display screen 21 changes by changing the area of the non display regions 312 (when the number of the image display regions 311 is one) (drawing 42 (a2) is darker than drawing 42 (a1), and drawing 42 (a3) is darker than drawing 42 (a2)).
[0325]Similarly, in the case of drawing 38 (b), drawing 42 (b2) is darker than drawing 42 (b1) (when the number of the image display regions 311 is two), and, in drawing 42 (b3), the display luminance of the display screen 21 becomes dark from drawing 42 (b2). The same may be said of the case (3 or more [when the number of the image display regions 311 is three that is,]) of drawing 38 (c) (drawing 42 (c2) is darker than drawing 42 (c1), and drawing 42 (c3) becomes dark from drawing 42 (c2)).
[0326]Although it presupposed that the image display region 311 scans the display screen 21 top in

drawing 38, An one-frame (1 field) eye makes the full screen the non display regions 312, and the following two-frame (2 field) eye is good also considering the full screen as the image display region 311 so that it may illustrate to not the thing limited to this but drawing 42 (c1), and (c2). That is, an image display state and an astigmatism light state are repeated for the full screen by turns. However, image display time and astigmatism light time are not limited to isochronous. For example, image display time is set to 1F/4, and it is good also considering astigmatism light time as 3F/4. Thus, the display luminance of a picture can be changed also by changing the rate of image display time and astigmatism light time (adjustment).

[0327]Anyway, as shown in drawing 43, the display luminance B of a picture can be linearly changed by changing the value of N. The luminosity of a picture is easily changed only by controlling the value of N.

[0328]Drawing 44 is a block diagram of the circuit which adjusts the display luminance of this invention (control). The picture image data inputted from the outside is accumulated in the frame memory (field memory) 354. CPU353 calculates using the accumulated picture image data. An operation uses at least one or more of the maximum luminance of picture image data, optimal brightness, average luminance, and luminance distribution. The maximum luminance of each frame of continuous picture image data, optimal brightness, average luminance, luminance distribution, and its changing ratio are also taken into consideration.

[0329]The calculated result is stored in the luminance memory 352. It is the data which amended the luminosity of the picture in the luminance memory 352. For example, on bright screens, such as the seashore, when the average luminance of a picture is amended brightly and there is a comparatively dark portion within the image data, it changes into image data actually darker than a value. In the screen of night, since it is dark on the whole, a picture amends a comparatively bright portion more brightly.

[0330]It is a circuit which counts how much the counter circuit 351 makes N-ary of drawing 43. In the waveform of the gate signal line 17b, N-ary is changed in real time. Since N-ary is time, by counting at a counter, it can be changed easily and can change the luminosity of a picture.

[0331]The switching circuit 355 is a circuit which changes the voltage Vgl which makes TFT11 of the pixel 16 one, and the voltage Vgh (it is a case where pixel TFT11 is P channel, and is the reverse by N channel) made to turn off. That is, based on the output of the counter circuit 351, the period of 1 F/N shown in drawing 37 (b) is changed. Therefore, the luminosity of the display screen 21 can be easily changed in real time.

[0332]Display luminance is controlled by real time according to video signal data. By controlling in this way, the dynamic range of luminosity expression is expandable to 3 or more times on parenchyma. Since an EL display serves as a black display (astigmatism light) thoroughly when not sending current through an EL element, the black float of image display does not generate it, either. That is, contrast also becomes high. Since the current value programmed to a pixel in a black display is as small as 10nA especially in the case of current programming, it is difficult to be unable to carry out the charge and discharge of the parasitic capacitance 404 enough, but to realize a perfect black display. Electric power is supplied to the source signal line 18 by the pulse impressed to the gate signal line 17 (running voltage), and it is generated by the black float.

[0333]It suspends that this invention turns OFF TFT11d for switching compulsorily, and supplies current to EL element 15. Therefore, EL element 15 will be in an astigmatism light state thoroughly. Therefore, good contrast is realizable.

[0334]In drawing 44, based on the picture image data of a video signal although the luminosity of a picture is changed in real time, it is not limited to this. For example, when a user pushes a lightness adjustment switch or turns a brightness adjusting volume, this change may be detected, the counter value of the counter circuit 351 may be changed, and the luminosity (or contrast or a dynamic range) of the display screen 21 may be changed. Photosensor may detect luminosities, such as outdoor daylight, and the luminosity of the display screen 21, etc. may be automatically changed based on this detected data. It may constitute so that it may be manual or may be made to change with the contents of the picture to display, and data automatically.

[0335]Lightness adjustment is realizable by making TFT (drawing 6 TFT11d for switching) by the side of EL element 15 turn on and off. In this case, the program current (voltage: in the case of a voltage program method) outputted from the source driver 14 is that which is a fixed value (program current is not changed), and can simplify the circuitry of a source driver. That is, it is because it is not necessary to change output current (voltage) etc. corresponding to the luminosity of a display screen. for example, -- the conventional liquid crystal display panel -- the time of 64 gradation displays -- the maximum luminosity -- eyes are used 64 gradation. When lowering luminosity by lightness adjustment rather than this, even eyes are used 32 gradation, for example. Thus, if a circuit is constituted, when screen intensity is

dark, the number of gradation displays will decrease.
[0336]A luminosity can be freely adjusted with adjustment of a "off" period also by the method which makes TFT11 by the side of EL element 15 turn on and off (the current which flows into EL element 15 is indicated by intermittent). In that case, the lightness adjustment by this invention can be held also in gamma adjustment and luminosity change of lineality. Since the power supply voltage Vdd is also a fixed value, a composition top is also advantageous.
[0337]The Gaussian distribution of the luminosity of a screen can be easily carried out by controlling an on-off state for TFT11d for switching down from on a screen. A calculation function is hardly needed also for controlling. This method will be explained later.
[0338]It is necessary to set to 0.5 or more msec the cycle which turns EL element 15 on and off. When this cycle was short, it will not be in a perfect black display state with the afterimage characteristic of human being's eyes, but a picture came to have faded, and resolution came to have fallen. Or it will be in the displaying condition of a data-hold type display panel. However, when an on-off cycle is set to 100 or more msec, it is visible to a flickering state. Therefore, the on-off cycle of the EL element should be made 100 or less msec of 0.5 or more msec, and 30 msec or less of 2 more or more msec. The on-off cycle should be made still more preferably 20 or less msec of 3 or more msec.
[0339]If it is set to one, it can realize good animation display, but since a flicker of a screen is in sight easily as for the number of partitions of the black picture (non display regions) 312, it is preferred to divide a black insert portion into plurality. However, since animation dotage will occur if the number of partitions is made too much large, the number of partitions should carry out to eight or less [1 or more]. Or more further 1 thing to do to five or less is preferred.
[0340]As for the number of partitions of a black picture, it is preferred to constitute so that it can change by the still picture and an animation. In N= 4, 75% is a black picture and 25% of the number of partitions is image display. At this time, the number of partitions 1 scans 75% of black indicator to the sliding direction of a screen in the state of 75% of black obi. It is the number of partitions 3 which is scanned at 3 blocks of 75% of black picture, and 25/3% of display screen. In the case of a still picture, the number of partitions is increased, and, in the case of an animation, the number of partitions is lessened. According to an inputted image, it may perform automatically (animation detection etc.), and a user may perform a change manually. What is necessary is just to constitute so that an input plug socket may be made to correspond and the image of a display, etc. may be changed.
[0341]For example, in a cellular phone etc., the number of partitions is made or more into ten in a wallpaper display and an input screen (it may turn on and off for everyH extremely). When displaying the animation of NTSC, the number of partitions is made or less [1 or more] into five. As for the number of partitions, it is preferred to constitute so that it can change to three or more multi stage stories. For example, it is number-of-partitions nothing, 2, 4, 8, etc.
[0342]As for the rate of a black picture over all the display screens, when area of the full screen is set to 1, it is preferred 0.2 or more things to do to 0.9 (it will be nine or less [1.2 or more] if it displays by N) or less, and to use 0.6 (if it displays by N, it will be six or less [1.25 or more]) or less [0.25 or more] especially. It is because the improvement effect in animation display is low in it being 0.20 or less. It is because the luminosity of a display portion becomes it high that it is 0.9 or more and it becomes that a display portion moves up and down that it is easy to be recognized visually.
[0343]As for the frame number per second, 100 (not less than 10 Hz 100 Hz or less) or less [10 or more] and 65 (not less than 12 Hz 65 Hz or less) or less [further 12 or more] are preferred. It is because the writing from the source driver 14 etc. will become painful and resolution will deteriorate, if a flicker of a screen comes to be conspicuous when there are few frame numbers, and there are too many frame numbers.
[0344]Anyway, as previously explained using drawing 37, drawing 44, etc., in this invention, control of the gate signal line 17 and change of the current (voltage) impressed to the source signal line 18 may perform, and it may carry out combining both.
[0345]It cannot be overemphasized that the above matter can also apply the pixel configuration of voltage programs, such as drawing 74 and drawing 76. For example, what is necessary is just to carry out on-off control of the TFT11e in drawing 74.
[0346]Any time may be sufficient as the time which makes only the period of 1 F/N of the gate signal line 17b ON state voltage Vgl among 1F (it may not be limited to 1F and an unit time period may be sufficient) periods so that it may illustrate to drawing 45. When only a predetermined period makes EL element 15 the one among unit time periods, it is because it is what obtains predetermined average luminance. However, since the direction which makes the gate signal line 17b ON state voltage Vgl immediately, and makes EL

element 15 emit light after the program period (1H) of drawing 45 (a) becomes difficult to be influenced by the retention characteristic of the capacitor 19 of drawing 6, it is good. In drawing 45 (b), as the sign and arrow of A and B show, the period of one F/N may be constituted so that a position may be changed. This change is also easily realizable, if it constitutes so that timing (when [of 1F] is L level used?) of the data impressed to ST in drawing 10 may be adjusted or changed.

[0347]The period (1 F/N) which makes the gate signal line 17b ON state voltage Vgl may be divided into plurality so that it may illustrate to drawing 46 (number of partitions K). That is, the period made into ON state voltage Vgl carries out the period of 1F/(K/N) K times. If it controls in this way, an image display state will serve as drawing 38 (b), (K= 2), and drawing 38 (c) and (K= 3). Thus, by dividing into plurality the picture part (image display region 311) made to turn on, generating of a flicker can be controlled and image display of a low frame rate can be realized. It is preferred to constitute so that the number of partitions of this picture may also be changed. For example, it may constitute so that it may be manual or may be made to change with the contents of the picture to display, and data automatically, as a user detects this change and changes the value of K by pushing a lightness adjustment switch or turning a brightness adjusting volume.

[0348]Thus, if it constitutes so that timing (when [of 1F] is L level used?) of the data impressed to ST in drawing 10 may be adjusted or changed, it is also easily realizable to change the value (number of partitions of the image display region 311) of K.

[0349]In drawing 46, the period (1 F/N) which makes the gate signal line 17b ON state voltage Vgl is divided into plurality (number of partitions K), and although the period made into ON state voltage Vgl presupposed that 1F / (K/N) period is carried out K times, it is not limited to this. L (L!=K) time operation of the 1F/(K/N) period may be carried out. That is, since this invention displays the display screen 21 by controlling the period (time) passed to EL element 15, carrying out L (L!=K) time operation of the period of 1F/(K/N) is included in the technical idea of this invention. The luminosity of the display screen 21 can be changed in digital one by changing the value of L. For example, in L= 2 and L= 3, 50% of luminosity (contrast) change is made. These control is also easily realizable by circuitry, such as drawing 10, drawing 44, drawing 55, and drawing 56.

[0350]When dividing the image display region 311, the period which makes the gate signal line 17b ON state voltage Vgl is not limited to the same period. For example, as shown in drawing 47, it is good also as two or more periods like t1 and t2 in the period made into ON state voltage Vgl.

[0351]In drawing 37, it illustrated so that the pixel row which adjoined might be made to turn on one by one (display), but this invention is not limited to this. Interlace scanning may be carried out so that it may illustrate to drawing 48. This interlace scanning is an image display method which writes a picture in an odd number pixel row (drawing 48 (a) write-in pixel row 391), and writes a picture in an even number pixel row in the 2nd next field (drawing 48 (b) write-in pixel row 391) in the 1st field. The pixel row which is not written in holds the image data of the front field (maintenance pixel row 392). Thus, a flicker can be decreased by carrying out interlace scanning with an EL display.

[0352]If it is a drive method of this drawing 48, the gate signal line 17b of all the even number pixel rows (or plurality) can be shared, and the gate signal line 17b of all the odd number pixel rows (or plurality) can be shared. Therefore, the number of leading about of the gate signal line 17 is substantially reducible. When displaying the image display region 311 and the non display regions 312 for the full screen by turns, all the gate signal lines 17b can be shared. These composition is effective with especially composition without three sides, such as drawing 13.

[0353]Although interlace scanning presupposed that a picture is written in an odd number pixel row, and a picture is written in an even number pixel row in the 2nd next field in the 1st field, it is not limited to this. the 1st field -- a 2-pixel line -- it may fly and come out, and may write in two pixel rows of pictures at a time, and a picture may also be written in every 2 which were not written in in the 1st field pixel rows in the 2nd next field. Three every pixel rows or four every pixel rows may be sufficient. In the 1st field, two pixel rows of pictures may be written in from each 2nd line of a screen (see drawing 49 (a)), and a picture may also be written in every two pixel rows from the 1st line in the 2nd next field (see drawing 49 (b)). The pixel row currently written in or the pixel row to write in may be controlled to become the non display regions 312 to illustrate to drawing 49. In the 1st field, a picture may be written in toward the bottom from on a screen, and a picture may also be written in toward a top from under a screen in the 2nd field. These are also all contained in the concept of interlace scanning.

[0354]Interlace scanning is also easily realizable by enforcing the method explained by drawing 37 and drawing 41. It is because the pixel row applicable to the non display regions 312 which are not made to turn on should just make TFT11d for switching shown in drawing 6 (a) turn off.

[0355]The non display regions 312 and interlace scanning are combinable so that it may illustrate to drawing 50 with a natural thing. In drawing 50 (a), the scan size 501 which consists of the write-in pixel row 391 and the maintenance pixel row 392 is shifted one by one. In drawing 50 (a), the picture is written in from the 1st line. Drawing 50 (b) also shifts the scan size 501 which consists of the write-in pixel row 391 and the maintenance pixel row 392 one by one in a similar manner. In drawing 50 (b), the picture is written in from the 2nd line.
[0356]The above example mainly explained the composition of the pixel 16 of drawing 6. However, this invention is not limited to this. For example, the pixel 16 of drawing 8 or drawing 9 is also realizable.
[0357]In the pixel configuration of drawing 8, the current value impressed to the source signal line 18 is programmed by the capacitor 19 by impressing ON state voltage Vgl to the gate signal line 17a. The data which corresponds to a video signal from the power supply switching means 403 in the source driver 14 is impressed to the source signal line 18 so that it may illustrate to drawing 51. When current mirror efficiency is 1, said current flows into TFT11b for a drive, and, as for the programmed current, this current is impressed to EL element 15. Probably, **** does not have these relations (timing waveform etc.) in explanation, since they can divert the matter illustrated to drawing 37 or are similar. However, when performing current programming, one or OFF timing of TFT11c for taking in and TFT11d for switching may have to be controlled individually. In this case, the gate terminal which makes TFT11c for taking in and TFT11d for switching turn on and off must be made into another gate signal line 17.
[0358]In order to enforce the methods of presentation, such as drawing 38, it is necessary to intercept the current sent through EL element 15. TFT11e is added so that it may illustrate to drawing 51 for the purpose of this interception. By making the gate terminal of TFT11e into ON state voltage Vgl, current is impressed to EL element 15 and the current to EL element 15 is intercepted by making the gate terminal of TFT11e into OFF state voltage Vgh (astigmatism light state).
[0359]Therefore, the image display explained by drawing 38 etc. is realizable by impressing the signal wave form of the gate signal lines 17a and 17b explained by drawing 37 etc.
[0360]The image display region 311 and the non display regions 312 may change an odd number pixel row and an even number pixel row to every frame (field) so that it may illustrate to drawing 52. An odd number pixel row is displayed by drawing 52 (a), with non-display, then the following frame (field) (see drawing 52 (b)), an odd number pixel row is made non-display for an even number pixel row, and an even number pixel row is displayed.
[0361]Thus, if it displays so that non display regions and a viewing area may be repeated for every pixel row, generating of a flicker will be controlled substantially.
[0362]In drawing 52, although a non-display pixel row and a display pixel line are used for every pixel row, though it is not limited to this and made a non-display pixel row and a display pixel line for every pixel row beyond every two pixel rows or it, it is good.
[0363]For example, if it is every two lines, if 1 pixel-row eye and 2 pixel-row eye are made into a display pixel line and 3 pixel-row eye and 4 pixel-row eye are made into a non-display pixel row, 5 pixel-row eye and 6 pixel-row eye will serve as a display pixel line in the 1st field (frame). In the 2nd next field (frame), if 1 pixel-row eye and 2 pixel-row eye are made into a non-display pixel row and 3 pixel-row eye and 4 pixel-row eye are made into a display pixel line, 5 pixel-row eye and 6 pixel-row eye will serve as a non-display pixel row. In the 3rd next field (frame), if 1 pixel-row eye and 2 pixel-row eye are made into a display pixel line and 3 pixel-row eye and 4 pixel-row eye are made into a non-display pixel row like the 1st field, 5 pixel-row eye and 6 pixel-row eye will serve as a display pixel line.
[0364]Wording of the field and a frame is used for homonymy, or this specification has separated it. Generally, in the interlace driving of NTSC, one frame comprises the 2 fields. However, in a progressive drive, one frame is the 1 field. Thus, although the field and a frame are properly used in the world of the signal of an image, the picture displayed on the display panel in this invention can apply progressive, an interlace, or either. Therefore, it is considered as expression that whichever may be sufficient. It is a unit of time to finish writing a series of screens notionally also with the field or a frame.
[0365]The method of presentation of drawing 53 is also effective. In order to explain easily here, make the 2nd field (the 2nd frame) and drawing 53 (c) into the 3rd field (the 3rd frame), and let [drawing 53 (a)] drawing 53 (d) be the 4th field (the 4th frame) for the 1st field (the 1st frame) and drawing 53 (b).
[0366]In the 1st field (frame), make 1 pixel-row eye and 2 pixel-row eye into a non-display pixel row, and let a display pixel line, 5 pixel-row eye, and 6 pixel-row eye be display pixel lines for 3 pixel-row eye and 4 pixel-row eye. In the 2nd field (frame), make an odd number pixel row eye into a display pixel line, and let an even number pixel row eye be a non-display pixel row. In the 3rd field (frame), make 1 pixel-row eye and 2 pixel-row eye into a display pixel line, and let 3 pixel-row eye and 4 pixel-row eye be non-display pixel

rows. In the 4th field (frame), make an odd number pixel row eye into a non-display pixel row, and let an even number pixel row eye be a display pixel line. Henceforth, it repeats successively from the displaying condition of the 1st field (the 1st frame).
[0367]In the drive method of drawing 53, it is considered as one loop in the 4 field (frame). Thus, generating of a flicker is controlled rather than drawing 52 by performing image display in plural fields (multiple frame) in many cases.
[0368]In the example of drawing 53, in the 1st field (frame), it is considered as 2 pixel-row eye [every] non-display pixel row, and although it was considered as 1 pixel-row eye [every] non-display pixel row, it is not limited to this in the 2nd field (frame). In the 1st field (frame), consider it as 4 pixel-row eye [every] non-display pixel row, and in the 2nd field (frame). Consider it as 2 pixel-row eye [every] non-display pixel row, and in the 3rd field (frame). It is considered as 1 pixel-row eye [every] non-display pixel row, is considered as 4 pixel-row eye [every] non-display pixel row in the 4th field (frame), is considered as 2 pixel-row eye [every] non-display pixel row in the 5th field (frame), and is good also as a 1 pixel-row eye [every] non-display pixel row in the 6th field (frame).
[0369]The drive method of this invention is easy to realize display effects (animation effect etc.). Drawing 54 is the method of presentation with which a viewing area appears one by one with drawing 54 (a) -> drawing 54 (b) -> drawing 54 (c) -> drawing 54 (d). An animation effect is realizable by scrolling the non display regions 312 slowly. Circuitry, such as drawing 10, drawing 55, and drawing 56, can also realize these control easily. This did not write in a black display state as an image, but has realized the animation effect easily by control of the gate signal line 17b etc.
[0370]The display panel which holds 1 field (one frame) period data to pixels, such as a liquid crystal display panel, has the technical problem that animation dotage occurs. However, since CRT is only displayed with an electron gun for a moment, the problem of animation dotage is not generated.
[0371]A means effective in solving this technical problem is black insertion. This invention can realize easily the black insertion method near CRT which reached to an extreme of animation display.
[0372]Drawing 57 shows the place where the character F moves downward from on a screen. The non-display state (drawing 57 (b), (d), (f)) is inserted between image display (drawing 57 (a), (c), (e)) so that it may illustrate to drawing 57. Therefore, a picture serves as a discontinuous display. Therefore, animation dotage does not occur but good animation display can be realized.
[0373]Thus, what is necessary is just to adopt the circuitry of drawing 55 for making the full screen into non display regions. The difference with drawing 10 is the point of providing the ENBL terminal 601. The ENBL terminal 601 is connected to one terminal of OR circuit 602 in which the gate signal line 17 was formed. By using an ENBL terminal as L level, a Vgh level will be outputted to all the gate signal lines 17b, TFT11d for switching or TFT11e which supplies current to EL element 15 will be in an OFF state, and the full screen serves as the non display regions 312. Normal operation is carried out when an ENBL terminal is H level.
[0374]Although drawing 10, drawing 55, drawing 56, and drawing 58 explained the data inputted into ST terminal as shifting one by one with the clock (serial operation), it is not limited to this. For example, it may be a parallel input which determines the on-off state of each gate signal line at once (the one OFUFU logic of all the gate signal line is a part for the number of a controller or the gate signal line 17, the composition which are outputted at once and for which it opts, etc.).
[0375]Although the example of drawing 57 was animation display, operation of an animation effect, such as carrying out flash plate INGU, is also easy for every R, G, and B (refer to drawing 59). As for the picture of the red display 311R, and drawing 59 (c), in drawing 59, the picture of the green display 311G and drawing 59 (e) of drawing 59 (a) are the pictures of the blue display 311B. The non-display state (drawing 59 (b), (d), (f)) is inserted between each picture of drawing 59 (a), (c), and (e). If operation from drawing 59 (a) to drawing 59 (f) is carried out slowly, this operation can be displayed as the picture of R, G, and B is carrying out flash plate INGU.
[0376]Like drawing 60, operation of a different animation effect, such as carrying out flash plate INGU for every picture, is also easy. As for the 1st picture 311a and drawing 60 (c), in drawing 60, the 2nd picture 311b and drawing 60 (e) of drawing 60 (a) are the 3rd picture 311c. The non-display state (drawing 60 (b), (d), (f)) is inserted between each picture of drawing 60 (a), (c), and (e). If operation from drawing 60 (a) to drawing 60 (f) is carried out slowly, it can display as the 1st, 2nd, and 3rd picture is carrying out flash plate INGU.
[0377]The above example is the method (Elements of the Invention) of sending N times as much current to the predetermined value of the source signal line 18 notionally, and only the period of 1/N sending N times as much current through EL element 15, and obtaining desired luminosity. By this method (Elements of the

Invention), the technical problem of the writing shortage by existence of the parasitic capacitance 404 was solved.
[0378]Luminous efficiency of the drive method increased N times improves rather than the time of 1 time (the conventional drive system). the direction which TFT11b for a drive of drawing 6 (capacitor 19 side) runs through this, it is influence of voltage, and is increased N times -- this -- it runs and the influence of voltage can be reduced. Eight or less times 1.5 or more-time are suitable for N multiple. As for N multiple, since the luminous efficiency of an EL element falls that it is more than this and the efficiency as the whole also falls, more than twice as many 6 or less times as this are preferred. Here, I hear that a light emission period is carried out to increasing N times at 1/N, and it is. Therefore, it will be said that a light emission period is carried out to making N multiple into 6 or less times more than twice 1/6 or less [1/2 or more] (at the time of the usual luminosity).
[0379]After this invention makes TFT11d for switching turn off and intercepts the current to EL element 15, it can send current through EL element 15 like the point by making TFT11d for switching one again. This invention applied this principle well, sent current during the 1/N, and has obtained predetermined luminosity. Thus, it can drive because the current value to pass is held every pixel 16 at the capacitor 19. That is, it can be said that this invention has applied well the pixel configuration peculiar to an EL display panel while holding the current value passed to EL element 15.
[0380](Embodiment 7) The composition of drawing 61 is the method of solving the technical problem of the writing shortage by existence of the parasitic capacitance 404, when driving ability forms N-1 time as many TFT11an for a drive to TFT11a for a drive.
[0381]The difference between drawing 61 and drawing 6 (a) is the point of having added N-1 time as many TFT11an-1 for a drive and TFT11f for switching other than TFT11a for a drive. It explains focusing on the difference between drawing 6 and drawing 61. It was referred to as TFT11an-1 for a drive because it constituted so that it might increase N times when the current of TFT11an-1 for a drive and TFT11a for a drive was added. That is, I hear that the channel width W2 of TFT11an-1 for a drive is increased N-1 time of the channel width W1 of TFT11a for a drive, and it is. For example, it will be N= 10, and if the channel width W1 of TFT11a for a drive sets to 1, it will be 9 times the channel width W2 of TFT11an-1 for a drive of this. Therefore, theoretically, if TFT11a for a drive sends the current of 1, it will be said that TFT11an-1 for a drive has the capability to send 9 times as much current.
[0382]When sending N times as much current through the source signal line 18, the driving current of TFT11an-1 for a drive was set to N-1 with the composition of drawing 61 by drawing 61 because 1 time as much current as TFT11a for a drive which sends current was added to EL element 15. In the composition of drawing 62, since the current of TFT11b for a drive which sends current through EL element 15 does not flow into the source signal line 18, it needs to increase driving current of TFT11n N times.
[0383]In order to explain easily here, TFT11a for a drive presupposes that the current which becomes I1 is sent, and supposing TFT11an-1 for a drive sends the current of In-1, a formula called I1+In-1=Iw (in this case, Iw carries out by N times the current I1 sent through EL element 15) will be realized.
[0384]During the current programming, the gate signal line 17a will be impressed to ON state voltage Vgl, and TFT11b for a drive, TFT11f for switching, and TFT11c for taking in will be in an ON state. OFF state voltage Vgh will be impressed to the gate signal line 17b, and TFT11d for switching will be in an OFF state. Therefore, the voltage equivalent to the program current Iw is programmed by the capacitor 19. that is, I1+In-1=Iw (in this case, Iw carries out by N times the current I1 sent through EL element 15) -- current flows into the source signal line 18.
[0385]Next, in the period which sends current through EL element 15, OFF state voltage Vgh will be impressed to the gate signal line 17a, and TFT11b for a drive, TFT11f for switching, and TFT11c for taking in will be in an OFF state. Therefore, the source signal line 18 and the pixel 16 are separated. ON state voltage Vgl will be impressed to the gate signal line 17b, and TFT11d for switching will be in an ON state. Therefore, the current I1 corresponding to 1/N of the program current Iw flows into EL element 15.
[0386]By driving as mentioned above, N times as much current as the current (current sent through an EL element) of a desired value can be sent through the source signal line 18. Therefore, the influence of the parasitic capacitance 404 is excepted and current programming can fully be performed to the capacitor 19. On the other hand, the current of a desired value can be impressed to EL element 15.
[0387]In drawing 61, although TFT11an-1 for a drive with the current capability of N-1 is produced to one pixel, it is not limited to this. As shown in drawing 63, two or more TFT(s) (drawing 63 TFT11n1-TFT11n6) may be produced. Since operation is the same as that of drawing 61, explanation is omitted.
[0388]The composition of drawing 61 can be developed also in the current mirror method illustrated to drawing 8. What is necessary is just to form TFT11n which has N times as much driving ability so that it

may illustrate to drawing 62. However, TFT11f for switching by current mirror composition does not have necessity.

[0389]In drawing 62, the ratio of the channel width W2 of TFT11n and the channel width W1 of TFT11b for a drive is set to N:1. In order to explain easily here, TFT11b for a drive presupposes that the current which becomes I1 is sent, and supposing TFT11n sends the current of In, it will serve as In=Iw (in this case, Iw carries out by N times the current I1 sent through EL element 15).

[0390]During the current programming, ON state voltage Vgl will be impressed to the gate signal line 17a, and TFT11c for taking in and TFT11d for switching will be in an ON state. Therefore, the voltage equivalent to the program current Iw is programmed by the capacitor 19. that is, -- In=Iw (in this case, Iw carries out by N times the current I1 sent through EL element 15) -- current flows into the source signal line 18. As for a little TFT11c for taking in, and TFT11d for switching, it is preferred to be able to shift timing and to control an on-off state. In this case, it is necessary to make separate the gate signal line which controls TFT11c for taking in, and the gate signal line which controls TFT11d for switching, and to carry out independent control.

[0391]Next, in the period which sends current through EL element 15, OFF state voltage Vgh will be impressed to the gate signal line 17a, and TFT11c for taking in and TFT11d for switching will be in an OFF state. Therefore, the source signal line 18 and the pixel 16 are separated, and the current I1 corresponding to 1/N of the program current Iw flows into EL element 15.

[0392]By driving as mentioned above, N times as much current as the current (current sent through an EL element) of a desired value can be sent through the source signal line 18. Therefore, the influence of the parasitic capacitance 404 is excepted and current programming can fully be performed to the capacitor 19. On the other hand, the current of a desired value can be impressed to EL element 15.

[0393]The gate signal line 17b and TFT11e are provided in order to control so that only the non image display of drawing 14 etc. or a 1/N period sends current through EL element 15 as drawing 51 explained. Therefore, in the composition of drawing 62, when a 1/N period carries out the pulse drive of the current which sends further N times as much current, and is sent through EL element 15, the problem of the writing shortage by the parasitic capacitance 404 is completely lost. A black insertion display can be realized easily and good animation display can be realized.

[0394]The composition of drawing 62 is dramatically effective. For example, with the composition of only drawing 6, if it is going to realize N= 10, it is necessary to impress 10 times as high pulse form current as a desired value to EL element 15. In this case, since the terminal voltage of EL element 15 becomes high, it is necessary to design Vdd voltage highly and, and EL element 15 may deteriorate.

[0395]However, in the composition of drawing 62, since it will be set to 5x2=10 if channel width W2 of TFT11n is made into 5 times of TFT11b for a drive and it programs with current high twice, if only one half of periods impress twice as many current as this to EL element 15, it is realizable. Therefore, the problem on which EL element 15 deteriorates does not have to be lost, either, and it is not necessary almost to make Vdd voltage high.

[0396]On the contrary, if it is going to realize N= 10 only by TFT11n, it is necessary to make channel width W2 of TFT11n into 10 times of TFT11b for a drive in the composition of drawing 62. If it increases 10 times, the forming face product of TFT11n occupies most area of a pixel. Therefore, a pixel numerical aperture becomes very small, or it becomes unrealizable. However, in the composition of drawing 62, since what is necessary is just to make channel width W2 of TFT11n into 5 times of TFT11b for a drive, sufficient pixel numerical aperture is realizable.

[0397]There are many realization methods of N= 10. For example, channel width W2 of TFT11n is made into twice TFT11b for a drive, They are how to carry out period impression of one fifth for 5 times higher current at EL element 15, how to make channel width W2 of TFT11n into 4 times of TFT11b for a drive, and carry out period impression of 1/2.5 for 2.5 times higher current at EL element 15, etc. That is, what is necessary is just to make it multiplication set to 10 in consideration of the design (channel width W2) of TFT11n, the current sent through EL element 15, and its period. Thus, the value of N can be designed freely.

[0398]In drawing 62, although TFT11n with the current capability of N is produced to one pixel, it is not limited to this. As shown in drawing 64, two or more TFT(s) (drawing 64 TFT11n1-TFT11n5) may be produced. Since operation is the same as that of drawing 62, explanation is omitted.

[0399]The composition of drawing 61 of there being many realization methods of N= 10 is also the same. Channel width W2 of TFT11an-1 for a drive is made into 4 times of TFT11a for a drive, They are how to carry out period impression of one half for current high twice at EL element 15, how to make channel width W2 of TFT11an-1 for a drive into twice TFT11a for a drive, and carry out period impression of one fifth for

5 times higher current at EL element 15, etc. That is, what is necessary is just to make it multiplication set to 10 in consideration of the design (channel width W2) of TFT11an-1 for a drive, the current sent through EL element 15, and its period. Thus, the value of N can be designed freely.

[0400]It is clear that the matter's explained above it is applicable also in drawing 61, drawing 63, drawing 65 - drawing 67. That is, this invention forms TFT for a drive with large channel width in each pixel, and increases the current which drives the source signal line 18. And as drawing 38 etc. explained, while increasing the current sent through EL element 15, it is the method or composition which makes a predetermined period the current sent through EL element 15.

[0401]The display explained by drawing 14, drawing 38, etc. is realizable by controlling turning on and off of TFT11d for switching, or TFT11e. Animation display can be improved and a luminosity can be adjusted with this display. Therefore, although it presupposed that the current which is proportional to an EL element at N times or N is impressed to EL element 15 in this invention, it is not limited to this. The composition of sending the current not more than 1 predetermined time or it through EL element 15 may be used. Even in this case, it is because the effect that animation display can be improved and a luminosity can be adjusted easily can be demonstrated.

[0402]Although drawing 6 and drawing 61 are also the same, when making TFT11d for switching into an ON state, characteristic dispersion by the kink phenomenon of TFT11a for a drive can be controlled by making resistance high. This explained with the composition of drawing 6 (b). Dispersion in the current which flows into TFT11a for a drive decreases by arranging TFT11e of drawing 6 (b) and impressing Vbb voltage (Vgl<Vbb<Vgh) to the gate terminal of TFT11e.

[0403]Therefore, also in the pixel configuration of drawing 6 and drawing 61, it is preferred to impress Vbb voltage to the gate signal line 17b, and to make TFT11d for switching one. That is, OFF state voltage Vgh is impressed in an OFF state, and TFT11d for switching impresses Vbb voltage in an ON state.

[0404]This control is easy if circuitry is carried out like drawing 56. It is because OFF state voltage Vgh is impressed to the gate signal line 17b in an OFF state and Vbb voltage can be impressed to the gate signal line 17b in an ON state, if the inverter of the output stage of the shift register 22b uses OFF state voltage Vgh and Vbb voltage as a power supply.

[0405]The method which controls each gate signal line 17 uniquely may be used for the on-off control of the gate signal line 17, without not being limited to this, although based on the data which the shift register 22 holds, and forming the shift register 22. For example, the arbitrary gate signal lines 17 which output ON state voltage may be chosen in a multiplexer circuit. It may be parallel and all the gate signal lines may be pulled out, and it may constitute so that ON state voltage or OFF state voltage can be freely impressed to each gate signal line. Thus, by constituting so that it may not be based on the held data of the shift register 22 but the arbitrary gate signal lines 17 can be chosen, Turning on and off of the display screens 21, such as drawing 34, drawing 35, drawing 38, drawing 42, Drawing 177, Drawing 180, Drawing 185, Drawing 188, and Drawing 190, or strength processing of luminance distribution becomes easy.

[0406]TFT11e which impresses Vbb voltage separately may be formed or arranged so that it may illustrate to drawing 65 like drawing 6 (b). The current mirror composition of this matter is also the same. For example, TFT11f for switching which impresses Vbb voltage may be separately formed or arranged so that it may illustrate to drawing 68 and drawing 69. The pixel configuration of drawing 70 is also the same.

[0407]In drawing 71, by dividing TFT11a for a drive into TFT11a1 and TFT11a2, and connecting a gate terminal to a cascade, a kink phenomenon can be controlled and characteristic dispersion can also be controlled. This is the same also about TFT11a for a drive of drawing 6, TFT11b for a drive of drawing 8, TFT11a for a drive of drawing 61, and TFT11b for a drive of drawing 62 (adopting as composition of TFT for a drive is preferred).

[0408]Although TFT11n etc. are divided into plurality in drawing 63 and drawing 64, What is necessary is just to control whether TFT11n1 and TFT11n2 which were divided as other composition so that it might illustrate to drawing 72 are operated as an object for driving current improvement by potential (Vgh or Vgl) impressed to the gate signal line 17c. If TFT11f2 is made into an OFF state, the current which flows into the source signal line 18 will be set to one half when TFT11n1 and TFT11n2 are operating. These control is good to determine from the image display data of a display panel, and a viewpoint of power consumption.

[0409]The difference between drawing 65 and drawing 66 is the point of having connected the gate terminal of TFT11f for switching to the gate signal line 17c. That is, the on-off state of TFT11f for switching is not influenced by the potential state of the gate signal line 17a, but it is in the point that original control is realizable. When TFT11f for switching is an OFF state continuously, TFT11n is in the state separated from the pixel, and serves as a pixel configuration of drawing 6 (a). If the gate signal line 17c and the gate signal line 17a are used short-circuiting in logic, it will become the composition of drawing

65.
[0410]The problem of drawing 65 here is a point that dispersion appears in the current which flows into EL element 15 for every pixel, when the characteristic gap of the threshold Vt of TFT11n and TFT11a for a drive, etc. has occurred for every pixel. If dispersion occurs on current, it will be rough also with uniform displays, such as a white raster, in a display image, and admiration will come out. In that respect, this problem is not generated with the composition of drawing 6.
[0411]Therefore, when the screen size of a display panel is small and there is little influence of the parasitic capacitance 404, TFT11f for switching is continuously used by an OFF state. The screen size of a display panel is large, and when influence of the parasitic capacitance 404 cannot be solved only in operation of TFT11a for a drive, it is good to make the gate signal line 17c short-circuit with the logic of the gate signal line 17a, and to drive by realizing the pixel configuration of drawing 65.
[0412]The circuit block which drives the pixel configuration of drawing 66 is shown in drawing 58. The shift register 22c which drives the gate signal line 17c is formed, and the gate signal line 17c is driven. When driving by the pixel configuration of drawing 6, the data of ST3 is continuously set to L, and to the gate signal line 17c, it controls continuously so that the OFF state voltage of Vgh is outputted. What is necessary is just to make the same the data input states (timing, logic, etc.) of the shift registers 22c and 22a, when using it with the composition of drawing 66.
[0413]The composition of this drawing 66 can also realize composition of a current mirror. The pixel configuration is shown in drawing 67. What is necessary is just to control whether divided TFT11a for a drive and TFT11n are operated as an object for driving current improvement by potential (Vgh or Vgl) impressed to the gate signal line 17c to illustrate to drawing 67. If TFT11f for switching is made into an OFF state, only the TFT11a for a drive will operate by the current which flows into the source signal line 18.
[0414]Therefore, when the screen size of a display panel is small and there is little influence of the parasitic capacitance 404 like the pixel configuration of drawing 66, TFT11f for switching is continuously used by an OFF state. The screen size of a display panel is large, and when influence of the parasitic capacitance 404 cannot be solved only in operation of TFT11a for a drive, the gate signal line 17c is made to short-circuit with the logic of the gate signal line 17a, driving current is increased, and it drives. Thus, also in the pixel configuration of drawing 67, the circuit block of drawing 58 is applicable.
[0415]The shift register 22c which controls the gate signal line 17c by composition of drawing 58 was formed newly, and was operated. However, it is not limited to this composition. Since Vgl or Vgh voltage is only impressed to the gate terminal of TFT11f for switching, the control logic of the gate signal line 17c is easy. What is necessary is just to impress OFF state voltage Vgh to the gate terminal of all the TFT11f for switching in the display screen 21, when not operating TFT11n. What is necessary is just to impress the potential of the gate signal line 17a to the gate signal line 17c, when operating TFT11n. Therefore, it is not necessary to use the shift register 22c separately like drawing 58. That is, it is because what is necessary is just to add a gate circuit so that the data of the shift register 22a may be outputted to the gate signal line 17c as it is or the potential of all the gate signal lines 17c may serve as OFF state voltage Vgh.
[0416](Embodiment 8) The drive method of this invention is explained below. By increasing the current sent through the source signal line 18 N times, the influence of the parasitic capacitance 404 is lost and good image display with resolution can be realized. Drawing 34 is an explanatory view of other examples which increase the current which flows into a source signal line. The drive method of this invention in drawing 34 is a method of choosing two or more pixel rows simultaneously fundamentally, carrying out the charge and discharge of the parasitic capacitance of a source signal line, etc. with the current with which the pixel row of these plurality was united, and improving current writing shortage substantially. Since two or more pixel rows will be simultaneously chosen if it is this drive method, the current which per pixel drives can be decreased and the current which flows into EL element 15 can also be decreased. Here, in order to explain easily, it explains as N= 10 as an example (the current sent through a source signal line is increased 10 times).
[0417]In this invention explained by drawing 34 etc., a pixel row chooses K pixel row simultaneously. From a source drivers IC, the N time current of predetermined current is impressed to the source signal line 18. N/K twice as many current as the current sent through an EL element is programmed by each pixel. In order to make an EL element into predetermined light emitting luminance, time to flow into an EL element is made into the K/N time of one frame. By driving in this way, the charge and discharge of the parasitic capacitance of the source signal line 18 can fully be carried out, and good resolution and predetermined light emitting luminance can be obtained.
[0418]That is, current is sent through an EL element, I hear that during the period of K/N of one frame

does not send current, and other periods (1F (N-1) K/N) have it. In this displaying condition, an image data display and a black display (astigmatism light) are repeatedly displayed for everyF, and an image data display will be in a discontinuous display (intermittent display) state in time. Therefore, outline dotage of a picture is lost and good animation display can be realized. Since it drives with N times as much current to the source signal line 18, it is not influenced by parasitic capacitance but can respond also to a high definition display panel.

[0419]First, in order to understand easily, as explained previously, one pixel row is chosen, and the method which programs N times as much current is explained, referring to a driving waveform etc. Drawing 73 is the explanatory view. In drawing 73, although the screen is illustrated oblong, it may not be limited to this, and it may be longwise, and other shape, such as a round shape, may be sufficient.

[0420]Drawing 73 (a) is illustrating the writing state to the display screen 21. In drawing 73 (a), 871 is a write-in pixel row. In drawing 73 (a), the number of the pixel rows written in 1H period is one. Although the pixel configuration of drawing 6 is mentioned as an example in the following examples and it explains, it may not be limited to this, and it may be a pixel configuration of current mirrors, such as drawing 8. It cannot be overemphasized that it is applicable also to the pixel configuration of voltage program methods, such as drawing 74, drawing 75, and drawing 76.

[0421]In drawing 73 (a), if the gate signal line 17a is chosen, the current which flows into the source signal line 18 will be programmed by TFT11a for conversion. At this time, OFF state voltage is impressed to the gate signal line 17b, and current does not flow into EL element 15. It is because this can have a seen capacity component of EL element 15 from the source signal line 18 in TFT11d for switching by the side of EL element 15 being an ON state, it is influenced by this capacity and current programming exact enough becomes impossible to the capacitor 19. Therefore, as drawing 73 (b) shows, the pixel row in which current is written serves as the non display regions 312. Since TFT11d for switching of other pixel rows is an ON state, it becomes the image display region 311. In the pixel configuration of the current mirror shown in drawing 8 etc., even if it is in the state where current flows into TFT11a for conversion which performs current programming, from the source signal line 18, EL element 15 is not visible. Therefore, it is not necessary to change into an astigmatism light state like drawing 73 (b). That is, it is not an indispensable condition of an invention like drawing 73 (b) to make a write-in pixel row into the non display regions 312.

[0422]Drawing 77 is a voltage waveform impressed to the gate signal line 17. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the chosen pixel row is indicated in the lower berth of drawing 77. (1) in a figure and (2) show the chosen pixel row number.

[0423]In drawing 77, the gate signal line 17a (1) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. This program current is N times (in order to explain easily, it explains as N= 10.) of a predetermined value. Of course, since predetermined values are data currents which display a picture, unless it is a white raster display etc., they are not a fixed value. It is. Therefore, it is programmed by the capacitor 19 so that 10 times as much current flows into TFT11a for conversion. When the pixel row (1) is chosen, OFF state voltage Vgh is impressed to the gate signal line 17b in the pixel configuration of drawing 6 (1), and current does not flow into EL element 15.

[0424]After 1H, the gate signal line 17a (2) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. This program current is N times (in order to explain easily, it explains as N= 10) the predetermined value. Therefore, it is programmed by the capacitor 19 so that 10 times as much current flows into TFT11a for conversion. When the pixel row (2) is chosen, in the pixel configuration of drawing 6, OFF state voltage Vgh is impressed to the gate signal line 17b (2), and current does not flow into EL element 15. However, since OFF state voltage Vgh is impressed to the gate signal line 17a (1) of a previous pixel row (1) and ON state voltage Vgl is impressed to the gate signal line 17b (1), it is a lighted condition.

[0425]After the following 1H, the gate signal line 17a (3) is chosen (Vgl voltage), OFF state voltage Vgh is impressed to the gate signal line 17b (3), and current does not flow into EL element 15 of a pixel row (3). However, since OFF state voltage Vgh is impressed to the gate signal line 17a (1) and (2) of a previous pixel row (1) and (2) and ON state voltage Vgl is impressed to the gate signal line 17b (1) and (2), it is a lighted condition.

[0426]Synchronizing with the synchronized signal of 1H, the picture is displayed for the above operation. However, 10 times as much current flows into EL element 15 in the drive system of drawing 77. Therefore, the display screen 21 is displayed by one about 10 times the luminosity of this. Of course, in order to perform a predetermined luminosity display in this state, it cannot be overemphasized that what is

necessary is just to make program current into 1/10. However, since writing shortage occurs with parasitic capacitance etc. that it is 1/10 of current, the fundamental main point of this invention programs with high current, and obtains predetermined luminosity by insertion of the non display regions 312.
[0427]However, the method of drawing 73 is also a category of this invention. That is, it is the concept that it is made for current higher than predetermined current to flow into EL element 15, and it fully carries out the charge and discharge of the parasitic capacitance of the source signal line 18. According to this, it becomes unnecessary to pass N times as much current to EL element 15. For example, a current route is formed in parallel with EL element 15, it may shunt that a dummy EL element is formed, this EL element forms a light-shielding film, and light is not made (emit) toward a straw-man EL element and EL element 15, and they may send current. [it] That is, when signal current is 0.2microA, program current is set to 2.2microA and 2.2microA is passed to TFT11a for conversion. 0.2micro of signal current A is sent through EL element 15 among this current, and 2microA is passed to a dummy EL element.
[0428]By constituting as mentioned above, by making the current sent through the source signal line 18 increase by N times, it can program and current sufficiently smaller than N times can be sent through current EL element 15 so that N times as much current may flow into TFT11a for conversion. without it forms the non display regions 312 in the above method so that it may illustrate to drawing 78 etc. -- drawing 73 -- like -- almost -- or all the display screens 21 can be thoroughly made into the image display region 311.
[0429]However, if workmanship of forming a straw-man EL element etc. is not carried out, the programmed current flows into EL element 15 theoretically [all]. Therefore, at drawing 73, a display screen emits light by one N times the luminosity of this. What is necessary is just to form the non display regions 312 so that it may illustrate to drawing 78 in order to make this emit light by predetermined luminosity. Drawing 78 is an explanatory view of the method.
[0430]Drawing 78 (a) is illustrating the writing state to the display screen 21. In drawing 78 (a), 871a is a write-in pixel row. Program current is supplied to each source signal line 18 from the source driver 14. In drawing 78, the number of the pixel rows written in 1H period is one. However, not the thing limited to 1H in any way but 0.5H period or 2H period may be sufficient. Although program current is written in the source signal line 18, the voltage program method of it not being limited to a current programming method and writing voltage in the source signal line 18 may be sufficient as this invention.
[0431]In drawing 78 (a), like drawing 73, if the gate signal line 17a is chosen, the current which flows into the source signal line 18 will be programmed by TFT11a for conversion. At this time, OFF state voltage is impressed and current does not flow through the gate signal line 17b into EL element 15. It is because this can have a seen capacity component of EL element 15 from the source signal line 18 in TFT11d for switching by the side of EL element 15 being an ON state, it is influenced by this capacity and current programming exact enough becomes impossible to the capacitor 19. Therefore, if composition of drawing 6 is made into an example, the pixel row in which current is written as drawing 78 (b) shows will serve as the non display regions 312.
[0432]What is necessary is just to let 90% of range of the display screen 21 be the non display regions 312, since the luminosity of a screen increases 10 times if programmed now with N times (here, referred to as N= 10 as stated previously) as much current. Therefore, what is necessary is to make 22 into the image display region 311, and just to 220-22=198 make it into the non display regions 312, if it is considered as 220 horizontal scanning lines of QCIF of an image display region (S= 220). If a horizontal scanning line (the number of pixel rows) is set to S, will make the field of S/N into the image display region 311, this image display region 311 will be made to emit light by one N times the luminosity of this and the sliding direction of a screen will be made to scan if it generally states, the field of S (N-1)/N will turn into the non display regions 312. These non display regions are black displays (nonluminescent). These non display regions 312 are realized by making TFT11d for switching turn off. Although it used making the light switch on by one N times the luminosity of this, one N times the value of this must be adjusted with lightness adjustment and gamma adjustment with a natural thing.
[0433]When programming with 10 times as much current by the previous example, the luminosity of the screen increased 10 times and presupposed that what is necessary is just to make 90% of range of the display screen 21 into the non display regions 312. However, this is not limited to making the pixel of RGB into the non display regions 312 in common. For example, the pixel of R may make one eighth the non display regions 312, the pixel of G may make one sixth the non display regions 312, and the pixel of B may be changed in each color so that 1/10 may be made into the non display regions 312. Although it may enable it to adjust the non display regions 312 (or image display region 311) individually by the color of RGB, in order to realize these, the individual gate signal line 17b is needed by R, G, and B. However, by

enabling individual adjustment of the above RGB, it becomes possible to adjust a white balance and the balance adjustment of a color becomes easy in each gradation.
[0434]A pixel row including the write-in pixel row 871a is made into the non display regions 312 so that it may illustrate to drawing 78 (b), Let the range of S/N of an upper screen be the image display region 311 rather than the write-in pixel row 871a (a write-in scan is a case down [from a screen], and it becomes the reverse when scanning a screen upwards from the bottom). The image display region 311 becomes band-like, and moves an image display state downward from on a screen.
[0435]Drawing 79 is a voltage waveform impressed to the gate signal line 17. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the chosen pixel row is indicated in the lower berth of drawing 79. (1) in a figure, (2), (3), and (4) show the chosen pixel row number.
[0436]In drawing 79, the gate signal line 17a (1) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. This program current is N times (in order to explain easily, it explains as N= 10.) of a predetermined value. Of course, since predetermined values are data currents which display a picture, unless it is a white raster display etc., they are not a fixed value. It is. Therefore, it is programmed by the capacitor 19 so that 10 times as much current flows into TFT11a for conversion. When the pixel row (1) is chosen, OFF state voltage Vgh is impressed to the gate signal line 17b in the pixel configuration of drawing 6 (1), and current does not flow into EL element 15.
[0437]After 1H (it is for explaining easily and not limited to 1H), the gate signal line 17a (2) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. This program current is N times (in order to explain easily, it explains as N= 10) the predetermined value. Therefore, it is programmed by the capacitor 19 so that 10 times as much current flows into TFT11a for conversion. At this time, ON state voltage Vgl is impressed to the gate signal line 17b (1). According to the example of drawing 78, the period when this ON state voltage is impressed is a period of S/N. Then, OFF state voltage Vgh is impressed to the gate signal line 17b (1), and current does not flow into EL element 15 of a pixel row (1).
[0438]When the pixel row (2) is chosen, OFF state voltage Vgh is impressed to the gate signal line 17b in the pixel configuration of drawing 6 (2), and current does not flow into EL element 15. However, since OFF state voltage Vgh is impressed to the gate signal line 17a (1) of a previous pixel row (1) and ON state voltage Vgl is impressed to the gate signal line 17b (1), it is a lighted condition. According to the example of drawing 78, the period when this ON state voltage is impressed is a period of S/N. Then, OFF state voltage Vgh is impressed and current does not flow through the gate signal line 17b (2) into EL element 15 of a pixel row (2).
[0439]After the following 1H, the gate signal line 17a (3) is chosen, OFF state voltage Vgh is impressed and current does not flow through the gate signal line 17b (3) into EL element 15 of a pixel row (3). However, since OFF state voltage Vgh is impressed to the gate signal line 17a (1) and (2) of a previous pixel row (1) and (2) and ON state voltage Vgl is impressed to the gate signal line 17b (1) and (2), it is a lighted condition. The above operation is repeated and the displaying condition of drawing 78 is realized.
[0440]In the display of drawing 78, the one image display region 311 moves to down from on a screen. If a frame rate is low, it will be recognized visually that the image display region 311 moves. It becomes that it is easy to be recognized when a palpebra is closed especially, or when moving a face up and down.
[0441]It is good to divide the image display region 311 into plurality so that it may illustrate to drawing 80 to this technical problem. Drawing 80 (b) is dividing the non display regions 312 into five. If the portion which added these five serves as area of S (N-1)/N, it will become equivalent to the luminosity of drawing 78. On the contrary, if it sees from the image display region 311, the image display region (lighting field) 311 is divided into six, but if it constitutes so that the portion which added the field divided into these six may be abbreviated-in agreement with S/N (drive), it will become equivalent to the display luminance of drawing 78.
[0442]It is not necessary to make equal the divided image display region 311 so that it may illustrate to drawing 80 (b). It is not necessary to also make equal the divided non display regions 312.
[0443]As mentioned above, by dividing the image display region 311 into plurality, a flicker of a screen decreases, there is no generating of a flicker, and good image display can be realized now. Although division may be made finer, the more it divides, the more animation display performance falls.
[0444]Drawing 81 is a voltage waveform impressed to the gate signal line 17. The difference between drawing 81 and drawing 79 is operation of the gate signal line 17b, and this gate signal line 17b carries out on-off (Vgl and Vgh) operation by that number corresponding to the number which divides a screen. Since

other points are the same as that of drawing 79, explanation is omitted.
[0445]In the above example, the pixel row chosen simultaneously was one pixel row. Drawing 35 is the method of choosing two or more pixel line simultaneously. By drawing 35, to explain choosing simultaneously with five pixel rows, in order to explain easily, but it is not limited to this and what is necessary is just two or more pixel rows. However, an increase of the pixel row chosen simultaneously will reduce the dispersion absorption effect of TFT11a for conversion.
[0446]Although explained by illustrating the pixel configuration of the current programming of drawing 6 also in the following examples, it is not limited to this. It cannot be overemphasized that it is effective also at the current mirror of drawing 8. When the pixel row chosen simultaneously increases, it is because charges and discharges, such as the parasitic capacitance 404 of a source signal line, become easy. The pixel configuration of voltage programs, such as drawing 75 and drawing 76, is also effective. When the pixel row chosen simultaneously increases, it is because the preliminary charging of the pixel row which adjoined can be carried out and it can respond also to a high definition display panel.
[0447]Current sent through the source signal line 18 from the source driver 14 in order to explain easily also here (or) The current which the source driver 14 absorbs from the source signal line 18, and the current which TFT11a for conversion slushes into the source signal line 18 explain as 10 times (N= 10) of a predetermined value. Therefore, if the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion will operate. That is, 10 per pixel / 5= 2 twice as many current as this flows into TFT11a for conversion. If the pixel rows chosen simultaneously are two pixel rows, the TFT11a for two conversion will operate. That is, it will be said that 10 per pixel / 2= 5 times as many current flows into TFT11a for conversion.
[0448]If the pixel rows chosen simultaneously are five pixel rows (K= 5), it will become what added five program current of TFT11a for conversion. For example, if the current to write in is originally set to Id and it is referred to as N= 10 at the write-in pixel row 871a, the current of Idx10 will be sent to the source signal line 18. The write-in pixel row 871b (871b is a pixel row used auxiliary in order to make the current amount to the source signal line 18 increase.) which adjoined the write-in pixel row 871a Therefore, the pixel (line) which writes in a picture is 871a, and in order to write in 871a, it is the pixel (line) 871b which is used auxiliary.
[0449]Ideally, TFT11a for 5-pixel conversion sends the current of Idx2 through the source signal line 18, respectively, and twice as many current as this comes to be programmed by the capacitor 19 of each pixel 16. However, actually, since the characteristic has shifted, dispersion generates each 5-pixel TFT11 on the current programmed by the capacitor 19 of each pixel. For example, 2.2 times, 2.0 times, 1.6 times, and 2.4 times as much current is respectively programmed by the write-in pixel row 871a at 1.8 times and the four write-in pixel rows 871b. In this example, 1.8 times as much current is programmed by the write-in pixel row 871a, and (2.0-1.8) / 2.0= 10% of error comes out. However, the current adding these is maintained at the default value of 10 times.
[0450]That is, the current according to characteristic dispersion flows into the selected pixel to the current programmed from the source driver 14 flowing into the source signal line 18 as regulation. Therefore, target program current will shift from a preset value, so that characteristic dispersion of TFT11a for conversion of each pixel is large. However, since the characteristic of adjoining TFT11a for conversion corresponds mostly, even if it makes the pixel row simultaneously chosen like drawing 35 increase, it can realize a uniform display.
[0451]Examples, such as drawing 34 and drawing 35, are more effective in the display panel which formed TFT11 with amorphous silicon art than the display panel which formed TFT11 with low-temperature-polysilicon art. In TFT11 of an amorphous silicon, it is because the characteristic of adjoining TFT is mostly in agreement. Therefore, even if it drives with the added current, the driving current of each TFT serves as a desired value mostly.
[0452]In drawing 35, if K line (K= 5) is simultaneously written in by the image data of the write-in pixel row 871a, the range of K line (871a, 871b) will serve as the same display. Thus, if the same display is used, resolution will fall with a natural thing. In order to cope with this, it writes in so that it may illustrate to drawing 35 (b), and let the portion of the pixel row 871 be the non display regions 312. Resolution lowering will not be generated if it does so.
[0453]After the following 1H, if the position which carried out 1 pixel-row shift is written in, the same operation is performed as the pixel row 871a and the 1-pixel (line) shift also of the non display regions 312 is carried out, the pixel (line) by which current programming was carried out by 1H of the point will be displayed.
[0454]The write-in pixel row 871b in which different current data from an original indicative data was

written when driven as mentioned above is not displayed, but if it shifts the above-mentioned operation of one line at a time, perfect image display is realizable. The charge and discharge of the parasitic capacitance 404 are also realizable within 1H period enough by the effect of the write-in pixel row 871b of using auxiliary.

[0455]Drawing 82 is an explanatory view of the driving waveform for realizing the drive method of drawing 35. Like drawing 77, a voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the chosen pixel row is indicated in the lower berth of drawing 82. (1), (2), (3) ... (6) shows the chosen pixel row number. In the case of a QCIF display panel, the number of lines is 220, and, in the case of the VGA panel, it is 480.

[0456]In drawing 82, the gate signal line 17a (1) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. Here, in order to explain easily, it explains first that the write-in pixel row 871a is eye pixel row (1) watch.

[0457]The program current which flows into the source signal line 18 is N times (in order to explain easily, it explains as N= 10.) of a predetermined value. Of course, since predetermined values are data currents which display a picture, unless it is a white raster display etc., they are not a fixed value. It is. It explains by making five pixel rows into simultaneous selection (K= 5). Therefore, ideally, it is programmed by the capacitor 19 of one pixel so that twice as many current as this flows into TFT11a for conversion.

[0458]When a write-in pixel row is (1) pixel-row eye, as illustrated by drawing 82, (1), (2), (3), (4), and (5) are chosen as the gate signal line 17a. That is, TFT11b for a drive of a pixel row (1), (2), (3), (4), and (5) and TFT11c for taking in are ON states. Since the gate signal line 17b serves as an opposite phase of the gate signal line 17a, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, current does not flow into corresponding EL element 15 of a pixel row, but it serves as the non display regions 312.

[0459]Ideally, TFT11a for 5-pixel conversion sends the current of Idx2 through the source signal line 18, respectively. And twice as many current as this is programmed by the capacitor 19 of each pixel 16. Here, in order to understand easily, it explains noting that the characteristic (Vt, S value) of each TFT11a for conversion corresponds.

[0460]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion operates. That is, 10 per pixel / 5= 2 twice as many current as this flows into TFT11a for conversion. The current which added five program current of TFT11a for conversion flows into the source signal line 18. For example, the current originally written in the write-in pixel row 871a is set to Id, and the current of Idx10 is sent through the source signal line 18. The write-in pixel row 871b which writes in image data henceforth from a write-in pixel row (1) is a pixel row used auxiliary in order to make the current amount to the source signal line 18 increase. However, since behind regular image data is written in, a problem does not have the write-in pixel row 871b.

[0461]Therefore, since it is the same display as the write-in pixel row 871a between 1H periods, the write-in pixel row 871b makes at least the write-in pixel row 871b chosen in order to make the write-in pixel row 871a and current increase the non display regions 312. However, in the pixel configuration of voltage program methods, such as a pixel configuration of a current mirror like drawing 8, and drawing 75, it is good also as a displaying condition depending on the case.

[0462]After the following 1H, the gate signal line 17a (1) serves as non selection, and ON state voltage Vgl is impressed to the gate signal line 17b (1). Simultaneously, the gate signal line 17a (6) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (6). By operating in this way, regular image data is held at a pixel row (1).

[0463]After the following 1H, the gate signal line 17a (2) serves as non selection, and ON state voltage Vgl is impressed to the gate signal line 17b (2). Simultaneously, the gate signal line 17a (7) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (7). By operating in this way, regular image data is held at a pixel row (2). One screen is rewritten by scanning, shifting one pixel row at a time with the above operation.

[0464]Although it is the same as that of drawing 73, in order to program with twice as many current (voltage) as this to each pixel, by the drive method of drawing 82, the light emitting luminance of EL element 15 of each pixel will be twice ideally. Therefore, the luminosity of a display screen will be twice rather than a predetermined value.

[0465]What is necessary is just to let one half of the ranges of the display screen 21 be the non display regions 312, including the write-in pixel row 871 so that you may illustrate to drawing 34 in order to make this into predetermined luminosity. Since it explained using drawing 79 etc., this is omitted.

[0466]Animation display performance improves, so that area of the black display area (non display regions)

312 occupied to the display screen 21 is enlarged. Therefore, what is necessary is to lessen the image display region 311 so that it may illustrate to drawing 83, and just to enlarge area of the non display regions 312.

[0467]Like drawing 34, the current programmed to each pixel can obtain predetermined display luminance, if the area of the image display region 311 is 1/2 of the display screen 21 in twice. However, like drawing 83, when the image display region 311 is smaller than one half of the display screens 21, a screen becomes dark. Then, what is necessary is just to enlarge the current programmed to each pixel, in order to obtain predetermined luminosity. For example, what is necessary is for the image display region (lighting field) 311 to be 1/5 of the area of the display screen 21, and just to increase the current (voltage) programmed to one pixel row 5 times of a predetermined value, if the number of the pixel rows chosen simultaneously is five (K= 5). The current which flows into the source signal line 18 will be 5x5 pixel-row =25 time.

[0468]Anyway, in the example of this invention, program current (voltage) can be adjusted by changing the current (voltage) sent through the source signal line 18. That is, I hear that the current which flows into the source signal line 18 can be adjusted only by adjusting the reference current (voltage) of the source driver 14, and it is. It can be set up by the data to ST* terminal impressed to the shift register 22 of the gate driver 12 illustrated to drawing 10 etc. whether five pixel rows are made whether two pixel rows are made one simultaneously or one simultaneously or only one pixel row is chosen. Therefore, the specification of the source driver 14 is not influenced by the pixel number to choose. Since the luminosity of a screen can also be adjusted by turning on and off of the gate signal line 17b, the output current from the source driver 14 is not changed by the lightness adjustment of the display screen 21. Therefore, what is necessary is just to determine the gamma characteristic of EL element 15 to one current. Therefore, the composition of the source driver 14 is very easy, and becomes a high thing of flexibility. The above matter is applicable also to the example of other this inventions.

[0469]If a frame rate is low like drawing 78 when the one image display region 311 moves to down from on a screen like drawing 83, it will be recognized visually that the image display region 311 moves. It becomes that it is easy to be recognized when a palpebra is closed especially, or when moving a face up and down.

[0470]It is good to divide the image display region 311 into plurality so that it may illustrate to drawing 84 to this technical problem. Drawing 84 (b) is dividing the non display regions 312 into three. If the portion which added these three serves as area of S (N-1)/N, it will become equivalent to the luminosity of drawing 83.

[0471]Drawing 85 is a voltage waveform impressed to the gate signal line 17. The difference between drawing 82 and drawing 85 is operation of the gate signal line 17b fundamentally. The gate signal line 17b carries out on-off (Vgl and Vgh) operation by the number corresponding to the number which divides a screen. Since other points can be almost the same as that of drawing 82 or can be guessed, they omit explanation.

[0472]The scanning direction of the non display regions 312 is not limited only to down from on a screen, and may be scanned above from under a screen so that it may illustrate to drawing 84 (b). The scanning direction from a top to the bottom and the scanning direction from the bottom to above may be scanned alternation or at random. It cannot be overemphasized that the number of partitions may be changed in the prescribed position of every frame or the display screen 21.

[0473]As mentioned above, by dividing the image display region 311 into plurality, a flicker of a screen decreases, does not have generating of a flicker, and can realize good image display now. Division may be made finer, and the more it divides, the more a flicker reduces it. Since especially the response of EL element 15 is quick, even if it turns on and off in time smaller than 5microsec, there is no fall of display luminance.

[0474]In the drive method of this invention, since turning on and off of EL element 15 is controllable by turning on and off of the signal impressed to the gate signal line 17b, a clock frequency is controllable by the low frequency of a KHz order. An image memory etc. are not needed when realizing black picture insertion (non-display-regions 312 insertion). Therefore, the drive circuit or method of this invention is realizable by low cost.

[0475]Drawing 86 is a case where the pixel rows chosen simultaneously are two pixel rows. According to the examined result, the method of choosing two pixel rows simultaneously in the display panel formed with low-temperature-polysilicon art had practical display uniformity. This is presumed because the characteristic of TFT11a for conversion of the pixel which adjoined is extremely in agreement. When carrying out laser annealing, the good result was obtained by irradiating with the direction of radiation of the laser of stripe shape in parallel with the source signal line 18.

[0476]In drawing 86, when a write-in pixel row is (1) pixel-row eye, as for the gate signal line 17a, (1) and

(2) are chosen (refer to drawing 87). At this time, TFT11b for a drive of a pixel row (1) and (2) and TFT11c for taking in are ON states. Since the gate signal line 17b serves as an opposite phase of the gate signal line 17a, TFT11d for switching of a pixel row (1) and (2) is an OFF state at least, and current is not flowing into corresponding EL element 15 of a pixel row. That is, it becomes the non display regions 312. In drawing 86, in order to reduce generating of a flicker, the image display region 311 is divided into five.

[0477]Ideally, TFT11a for 2 pixels (line) conversion sends the current of Idx5 (in the case of N= 10) through the source signal line 18, respectively, and 5 times as much current comes to be programmed by the capacitor 19 of each pixel 16.

[0478]Since the pixel rows chosen simultaneously are two pixel rows (K= 2), the TFT11a for two conversion operates. That is, 10 per pixel / 2= 5 times as many current flows into TFT11a for conversion, and the current which added two program current of TFT11a for conversion flows into the source signal line 18.

[0479]For example, the current originally written in the write-in pixel row 871a is set to Id, and the current of Idx10 is sent through the source signal line 18. Since behind regular image data is written in, a problem does not have the write-in pixel row 871b. Since it is the same display as the write-in pixel row 871a between 1H periods, the write-in pixel row 871b makes at least the write-in pixel row 871b chosen in order to make the write-in pixel row 871a and current increase the non display regions 312.

[0480]After the following 1H, the gate signal line 17a (1) serves as non selection, and ON state voltage Vgl is impressed to the gate signal line 17b (1). Simultaneously, the gate signal line 17a (3) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (3). By operating in this way, regular image data is held at a pixel row (1).

[0481]After the following 1H, the gate signal line 17a (2) serves as non selection, and ON state voltage Vgl is impressed to the gate signal line 17b (2). Simultaneously, the gate signal line 17a (4) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (4). By operating in this way, regular image data is held at a pixel row (2). One screen is rewritten by scanning, shifting one pixel row at a time with the above operation.

[0482]Although it is the same as that of drawing 51, in order to program with 5 times as much current (voltage) to each pixel, by the drive method of drawing 88, the light emitting luminance of EL element 15 of each pixel will be 5 times ideally. Therefore, the luminosity of the image display region 311 will be 5 times rather than a predetermined value. What is necessary is just to let one fifth of the ranges of the display screen 21 be the non display regions 312, including the write-in pixel row 871 so that you may illustrate to drawing 34 in order to make this into predetermined luminosity. Since it explained using drawing 79 etc., this is omitted.

[0483]In the drive method which chooses two or more pixel rows simultaneously, it becomes difficult to absorb characteristic dispersion of TFT11a for conversion, so that the number of pixel rows chosen simultaneously increases. However, if the current which the current programmed to 1 pixel becomes large, will send big current through EL element 15, and will be sent through EL element 15 if a selection number falls is large, EL element 15 will deteriorate easily.

[0484]Drawing 89 solves this technical problem. As drawing 35 explained, the fundamental concept of drawing 89 chooses two or more pixel rows simultaneously, and as drawing 73 explained, it combines the method of choosing one pixel row 1/2H (1/2 of a horizontal scanning period) by 1/2H (1/2 of a horizontal scanning period) of after that. By combining in this way, characteristic dispersion of TFT11a for conversion can be absorbed, and homogeneity within a field can be made good at high speed.

[0485]In drawing 89, in order to explain easily, in the 1st period, five pixel rows are chosen simultaneously, and in the 2nd period, it explains noting that one pixel row is chosen.

[0486]First, in the 1st period, five pixel rows are simultaneously chosen so that it may illustrate to drawing 89 (a1). This operation was explained using drawing 35. The current sent through a source signal line is made into 25 times of a predetermined value. Therefore, 5 times as much current is programmed by TFT11a for conversion of each pixel 16. And since it is 25 times as much current, the charge and discharge of the parasitic capacitance 404 are carried out extremely for a short period of time. Therefore, the potential of a source signal line turns into target potential for a short time, and it is programmed so that the terminal voltage of the capacitor 19 of each pixel 16 also sends 5 times as much current. Applying time of current is set to 1/2H (1/2 of one horizontal scanning period) these 25 times.

[0487]Since identical image data is written in 5 of the write-in pixel row 871 pixel rows with a natural thing, TFT11 is made into an OFF state in order to make it not display. Therefore, a displaying condition serves as drawing 89 (a2).

[0488]The 1/2H next period chooses one pixel row, and performs a current (voltage) program. This state is illustrated to drawing 89 (b1). The current (voltage) program of the write-in pixel row 871a is carried out so that 5 times as much current may be sent like the point. Here, the current sent through each pixel by drawing 89 (a1) and drawing 89 (b1) is made the same in order to make small change of the terminal voltage of the programmed capacitor 19 and to be able to send target current through a high speed more.
[0489]That is, by drawing 89 (a1), current is sent through two or more pixels, and it brings close to the value into which the current of an outline flows at high speed. In this 1st phase, since it is programming by two or more TFT11a for conversion, the error by dispersion in TFT has occurred to a desired value, but. Only the pixel row which writes in and holds data in the 2nd following phase is chosen, and a program perfect from the desired value of an outline to a predetermined desired value is performed.
[0490]Since it is the same as that of examples, such as drawing 34, drawing 35, and drawing 73, to scan the non display regions 312 down from on a screen, and to scan the write-in pixel row 871a down from on a screen, explanation is omitted.
[0491]Drawing 90 is a driving waveform for realizing the drive method of drawing 89. 1H (one horizontal scanning period) comprises two phases, and is changed by an ISEL signal so that it may understand by drawing 89. About the ISEL signal, it is illustrating to drawing 91.
[0492]First, the ISEL signal is explained. In drawing 91, the current output circuit 1222 comprises two, 1222a and 1222b. Each current output circuit 1222 comprises the DA circuit 1226, the operational amplifier 1224, etc. which carry out the DA translation of the 8-bit gradation data. Since the circuit operation of this current output circuit 1222 was explained previously, it omits. The current output circuit 1222a comprises an example of drawing 89 so that 25 times as much current may be outputted. On the other hand, the current output circuit 1222b is constituted so that 5 times as much current may be outputted. The switching circuit 1223 is controlled by an ISEL signal, and the output of the current output circuits 1222a and 1222b is impressed to the source signal line 18.
[0493]The current output circuit 1222a where an ISEL signal outputs current 25 times at the time of L level is chosen, and the source driver 14 absorbs the current from the source signal line 18. At the time of H level, the current output circuit 1222b which outputs current 5 times is chosen, and the source driver 14 absorbs the current from the source signal line 18. Thus, since what is necessary is just to change the value of the resistance 1228, the size change of current, such as 25 times and 5 times, is easy. It can change easily making resistance 1228 into BORIUMU, or by connecting with two or more resistance and an analog switch, and choosing.
[0494]As shown in drawing 90, when a write-in pixel row is (1) pixel-row eye (see the column of the pixel row number 1 of drawing 90), as for the gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, TFT11b for a drive of a pixel row (1), (2), (3), (4), and (5) and TFT11c for taking in are ON states. Since ISEL is L level, the current output circuit 1222a which outputs current 25 times is chosen, and it is connected with the source signal line 18. OFF state voltage Vgh is impressed to the gate signal line 17b. Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.
[0495]Ideally, TFT11a for 5-pixel conversion sends the current of Idx2 through the source signal line 18, respectively. And 5 times as much current is programmed by the capacitor 19 of each pixel 16. Here, in order to understand easily, it explains noting that the characteristic (Vt, S value) of each TFT11a for conversion corresponds.
[0496]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion operates. That is, 25 per pixel / 5= 5 times as many current flows into TFT11a for conversion. The current which added five program current of TFT11a for conversion flows into the source signal line 18. For example, the current originally written in the write-in pixel row 871a is set to Id, and the current of Idx25 is sent through the source signal line 18. The write-in pixel row 871b which writes in image data henceforth from a write-in pixel row (1) is a pixel row used auxiliary in order to make the current amount to the source signal line 18 increase. However, since behind regular image data is written in, a problem does not have the write-in pixel row 871b.
[0497]Therefore, the write-in pixel row 871b is the same display as the write-in pixel row 871a between 1H periods. Therefore, let at least the write-in pixel row 871b chosen in order to make the write-in pixel row 871a and current increase be the non display regions 312.
[0498]In the following 1/2H (1/2 of a horizontal scanning period), it is pixel-row [write-in] 871a Accepted, that is, only (1) pixel-row eye is chosen. ON state voltage Vgl is impressed to the gate signal line 17a (1), and OFF state voltage Vgh is impressed to the gate signal line 17a (2), (3), (4), and (5) so that clearly [in drawing 90]. Therefore, although TFT11a for conversion of a pixel row (1) is an operating state (state

which supplies current to the source signal line 18), TFT11b for a drive of a pixel row (2), (3), (4), and (5) and TFT11c for taking in are OFF states, i.e., a non selection state. Since ISEL is H level, the current output circuit 1222b which outputs current 5 times is chosen, and this current output circuit 1222b and source signal line 18 are connected. The state of the gate signal line 17b does not have a previous state of 1/2H, and change, and OFF state voltage Vgh is impressed. Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.

[0499]From the above thing, TFT11a for conversion of a pixel row (1) sends the current of Idx5 through the source signal line 18, respectively, and 5 times as much current is programmed by the capacitor 19 of each pixel row (1).

[0500]In the next horizontal scanning period, one pixel row and a write-in pixel row shift. That is, it is a time of a write-in pixel row being (2) shortly. In the first period of 1/2H, it writes in, as shown in drawing 90, and when a pixel row is (2) pixel-row eye, as for the gate signal line 17a, (2), (3), (4), (5), and (6) are chosen. That is, TFT11b for a drive of a pixel row (2), (3), (4), (5), and (6) and TFT11c for taking in are ON states. Since ISEL is L level, the current output circuit 1222a which outputs current 25 times is chosen, and it is connected with the source signal line 18. OFF state voltage Vgh is impressed to the gate signal line 17b (2), (3), (4), (5), and (6). Therefore, TFT11d for switching of a pixel row (2), (3), (4), (5), and (6) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312. On the other hand, since Vgl voltage is impressed, TFT11d for switching is an ON state, and EL element 15 of a pixel row (1) turns on the gate signal line 17b (1) of a pixel row (1).

[0501]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion operates. That is, 25 per pixel / 5= 5 times as many current flows into TFT11a for conversion. The current which added five program current of TFT11a for conversion flows into the source signal line 18.

[0502]In the following 1/2H (1/2 of a horizontal scanning period), only the write-in pixel row 871a is chosen. That is, only (2) pixel-row eye is chosen. ON state voltage Vgl is impressed to the gate signal line 17a (2), and OFF state voltage Vgh is impressed to the gate signal line 17a (3), (4), (5), and (6) so that clearly [in drawing 90]. Therefore, although TFT11a for conversion of a pixel row (1) and (2) is an operating state (state where a pixel row (1) sends current through EL element 15, and the pixel row (2) supplies current to the source signal line 18), TFT11b for a drive of a pixel row (3), (4), (5), and (6) and TFT11c for taking in are OFF states, i.e., a non selection state. Since ISEL is H level, the current output circuit 1222b which outputs current 5 times is chosen, and this current output circuit 1222b and source signal line 18 are connected. The state of the gate signal line 17b does not have a previous state of 1/2H, and change, and OFF state voltage Vgh is impressed. Therefore, TFT11d for switching of a pixel row (2), (3), (4), (5), and (6) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.

[0503]From the above thing, TFT11a for conversion of a pixel row (2) sends the current of Idx5 through the source signal line 18, respectively. And 5 times as much current is programmed by the capacitor 19 of each pixel row (2). One screen can be displayed by carrying out the above operation one by one.

[0504]The drive method explained by drawing 89 chooses G pixel row (G is two or more) in the 1st period, and programs it for each pixel row to send N times as much current. It is a method programmed to choose B pixel row (it is smaller than G and B is one or more) in the 2nd period after the 1st period, and to send N times as much current through a pixel.

[0505]However, there are other policies. G pixel row (G is two or more) is chosen in the 1st period, and it programs so that the total current of each pixel row turns into N times as much current. It is a method programmed so that B pixel row (it is smaller than G and B is one or more) will be chosen in the 2nd period after the 1st period and the current (current of one pixel row when [however,] a selected picture element line is 1) of total of the selected pixel row will be N times. For example, in drawing 89 (a1), if five pixel rows are chosen simultaneously and twice as many current as this is sent through TFT11a for conversion of each pixel, 5x2 times = 10 times as much current will flow into the source signal line 18. In the 2nd next period, in drawing 89 (b1), one pixel row is chosen and 10 times as much current is sent through this TFT11a 1 pixel for conversion.

[0506]If it is this method, like drawing 91, it is [two or more current output circuits 1222] less necessary, and they can constitute the source driver 14 from the one current output circuit 1222 in each source signal line. That is, the output current of the source driver 14 which sends the current of the source signal line 18 in this method is constant value (naturally this constant value changes with image data.). in this case, it is not based on the number of selected picture elements during 1H period, but means being fixed -

- it is . Therefore, the composition of the source driver 14 becomes easy.
[0507]In drawing 89, the period which chooses two or more pixel rows simultaneously is set to 1/2H, and although the period which chooses one pixel row was set to 1/2H, it is not limited to this. For example, it is good also considering the period which sets to 1/4H the period which chooses two or more pixel rows simultaneously, and chooses one pixel row as 3/4H. Although the period which added the period which chooses two or more pixel rows simultaneously, and the period which chooses one pixel row was set to 1H, it is not limited to this. For example, 2H period may also be 1.5H period.
[0508]In drawing 89, though the period which chooses five pixel rows simultaneously is set to 1/2H and two pixel rows are simultaneously chosen in the 2nd next period, it is good. Even in this case, convenient image display is realizable practically.
[0509]In drawing 89, the 1st period that chooses five pixel rows simultaneously is set to 1/2H, and although it was considered as two steps which set to 1/2H the 2nd period that chooses one pixel row, it is not limited to this. For example, it is good also as three stages which the 1st phase chooses five pixel rows simultaneously, and the 2nd period chooses two pixel rows among said five pixel rows, and finally choose one pixel row. That is, image data may also be written in a pixel row in two or more stages.
[0510]Although it presupposed that the two current output circuits 1222 are established in each source signal line 18 in drawing 91, since this outputs 25 times as much current to the 1st period that is the 1st example of drawing 89, it is for outputting 5 times as much current to the 2nd period. In order to realize this in the one current output circuit 1222, it is good to adopt the circuitry of drawing 88. The DA circuit 1226 carries out digital to analog by making the size of reference voltage (Iref) into the maximum. For example, if Iref voltage is 5V, the analog output of what divided 5V into 256 will be carried out as the minimum. That is, the maximum of an analog output is a 5V-1 bit analog value, the minimum is 0V, and the minimum resolution is 5V/256 (when an input is 8-bit specification). If Iref voltage is 2.5V, the analog output of what divided 2.5V into 256 will be carried out as the minimum. That is, the maximum of an analog output is a 2.5V-1 bit analog value, the minimum is 0V, and the minimum resolution is 2.5V/256 (when an input is 8-bit specification).
[0511]That is, an output current value can be changed by changing Iref voltage dynamically in the one current output circuit 1222. Drawing 88 is the realization circuit.
[0512]Resistance RI which quadrisects Vi voltage is provided in drawing 88. This voltage by which the partial pressure was carried out is inputted into the switching circuit 1223, one voltage is chosen, and it becomes Iref voltage. This Iref voltage is inputted into the operational amplifier 1224. Therefore, the magnification of output current can be changed by changing the Iref voltage of the period of 1/2H of the first half, and the Iref voltage of the period of 1/2H of the second half in the current output circuit 1222 where it was connected to all the source signal lines 18. Of course, Iref voltage may be generated by selection of two or more operational amplifiers 1224 so that it may illustrate to drawing 92.
[0513]Also in drawing 91, the image display region 311 is good also as one so that it may illustrate to drawing 93. It may divide into two or more image display regions 311 so that it may illustrate to drawing 94.
[0514]As illustrated to drawing 95, when a write-in pixel row is (1) pixel-row eye, as for the gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, TFT11b for a drive of a pixel row (1), (2), (3), (4), and (5) and TFT11c for taking in are ON states. Since ISEL is L level, the current output circuit 1222a which outputs current 25 times is chosen, and it is connected with the source signal line 18. OFF state voltage Vgh is impressed to the gate signal line 17b (1), (2), (3), (4), and (5). Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.
[0515]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion operates. That is, 25 per pixel / 5= 5 times as many current flows into TFT11a for conversion. The current which added five program current of TFT11a for conversion flows into the source signal line 18. For example, the current originally written in the write-in pixel row 871a is set to Id, and the current of Idx25 is sent through the source signal line 18. In order for the write-in pixel row 871b which writes in image data henceforth to make the current amount to the source signal line 18 increase from a write-in pixel row (1), it is a pixel row used auxiliary, but since behind regular image data is written in, a problem does not have the write-in pixel row 871b.
[0516]Therefore, the write-in pixel row 871b is the same display as the write-in pixel row 871a between 1H periods. Therefore, let at least the write-in pixel row 871b chosen in order to make the write-in pixel row 871a and current increase be the non display regions 312.
[0517]In the following 1/2H (1/2 of a horizontal scanning period), only the write-in pixel row 871a is chosen. That is, only (1) pixel-row eye is chosen. ON state voltage Vgl is impressed to the gate signal line

17a (1), and OFF state voltage Vgh is impressed to the gate signal line 17a (2), (3), (4), and (5). Therefore, although TFT11a for conversion of a pixel row (1) is an operating state (state which supplies current to the source signal line 18), TFT11b for a drive of a pixel row (2), (3), (4), and (5) and TFT11c for taking in are OFF states, i.e., a non selection state. Since ISEL is H level, the current output circuit 1222b which outputs current 5 times is chosen, and this current output circuit 1222b and source signal line 18 are connected. The state of the gate signal line 17b does not have a previous state of 1/2H, and change, and OFF state voltage Vgh is impressed. Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.

[0518]From the above thing, TFT11a for conversion of a pixel row (1) sends the current of Idx5 through the source signal line 18, respectively, and 5 times as much current is programmed by the capacitor 19 of each pixel row (1).

[0519]In the next horizontal scanning period, one pixel row and a write-in pixel row shift. That is, it is a time of a write-in pixel row being (2) shortly. As for the gate signal line 17a, in the first period of 1/2H, (2), (3), (4), (5), and (6) are chosen. That is, TFT11b for a drive of a pixel row (2), (3), (4), (5), and (6) and TFT11c for taking in are ON states. Since ISEL is L level, the current output circuit 1222a which outputs current 25 times is chosen, and it is connected with the source signal line 18. OFF state voltage Vgh is impressed to the gate signal line 17b (2), (3), (4), (5), and (6). Therefore, TFT11d for switching of a pixel row (2), (3), (4), (5), and (6) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312. On the other hand, since Vgl voltage is impressed to the gate signal line 17b (1) of a pixel row (1), TFT11d for switching is an ON state, and EL element 15 of a pixel row (1) is turned on.

[0520]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five conversion operates. That is, 25 per pixel / 5= 5 times as many current flows into TFT11a for conversion, and the current which added five program current of TFT11a for conversion flows into the source signal line 18.

[0521]In the following 1/2H (1/2 of a horizontal scanning period), only the write-in pixel row 871a is chosen. That is, only (2) pixel-row eye is chosen. ON state voltage Vgl is impressed to the gate signal line 17a (2), and OFF state voltage Vgh is impressed to the gate signal line 17a (3), (4), (5), and (6). Therefore, although TFT11a for conversion of a pixel row (1) and (2) is an operating state (state where a pixel row (1) sends current through EL element 15, and the pixel row (2) supplies current to the source signal line 18), TFT11b for a drive of a pixel row (3), (4), (5), and (6) and TFT11c for taking in are OFF states, i.e., a non selection state. Since ISEL is H level, the current output circuit 1222b which outputs current 5 times is chosen, and this current output circuit 1222b and source signal line 18 are connected. The state of the gate signal line 17b does not have a previous state of 1/2H, and change, and OFF state voltage Vgh is impressed. Therefore, TFT11d for switching of a pixel row (2), (3), (4), (5), and (6) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.

[0522]From the above thing, TFT11a for conversion of a pixel row (2) sends the current of Idx5 through the source signal line 18, respectively, and 5 times as much current is programmed by the capacitor 19 of each pixel row (2). One screen can be displayed by carrying out the above operation one by one.

[0523]Although the above explanation is also clear, the above-mentioned operation is the same as that of drawing 90. A difference is operation of the gate signal line 17b, and the gate signal line 17b carries out on-off (Vgl and Vgh) operation by the number corresponding to the number which divides a screen.

[0524]The scanning direction of the non display regions 312 is not limited only to down from on a screen so that it may illustrate also to drawing 94. It may scan above from under a screen. The scanning direction from a top to the bottom and the scanning direction from the bottom to above may be scanned alternation or at random. It cannot be overemphasized that the number of partitions may be changed in the prescribed position of every frame or the display screen 21.

[0525]As mentioned above, a flicker of a screen decreases by dividing the image display region 311 into plurality. Therefore, there is no generating of a flicker and good image display can be realized. Division may be made finer, and the more it divides, the more a flicker is reduced. Since especially the response of EL element 15 is quick, even if it turns on and off in time smaller than 5microsec, there is no fall of display luminance.

[0526]G pixel row (G is two or more) was chosen in the 1st period, and it programmed to send N times as much current through each pixel row, and in the 2nd period after the 1st period, B pixel row (it is smaller than G and B is one or more) was chosen, and the example of drawing 95 was also made into the method

programmed to send N times as much current through a pixel. However, there are other policies as well as drawing 90. That is, G pixel row (G is two or more) is chosen in the 1st period, and it programs so that the total current of each pixel row turns into N times as much current. It is a method programmed so that B pixel row (it is smaller than G and B is one or more) will be chosen in the 2nd period after the 1st period and the current (current of one pixel row when [however,] a selected picture element line is 1) of total of the selected pixel row will be N times.

[0527]The above example was the method of displaying a picture by sequential scanning. That is, if it says with a TV signal, it will be a non-interlaced drive (progressive drive). This invention is effective also in interlace driving. Drawing 96 is an explanatory view of interlace driving.

[0528]The number of interlace driving is usually one in the 2 fields. The 2 fields also explained drawing 96 as one frame (one screen). However, this is a case of the TV signal of NTSC and it is not necessary to necessarily keep a 2 field =1 frame principle in image display, such as a cellular phone.

[0529]For example, it is good also as one frame in the 4 field. The 1st field writes in Y-43 (Y is zero or more integers) pixel row, and the 2nd field writes in Y-42 (Y is zero or more integers) pixel row. The 3rd field writes in Y-41 (Y is zero or more integers) pixel row, and the 4th field is a method which writes in 4Y (Y is zero or more integers) pixel row. That is, interlace driving is the method of constituting one frame (one screen) from two or more fields.

[0530]Drawing 96 (a) is the 1st field and writes in an even number pixel row. Drawing 96 (b) is the 2nd field and writes in an odd number pixel row. Drawing 97 is a driving waveform for realizing the drive method of drawing 96. An odd number field and an even number field are the things on expedient. By drawing 96, it explains first writing in a picture from an odd number pixel row.

[0531]In drawing 96, the gate signal line 17a (1) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row. Here, in order to explain easily, it explains first that the write-in pixel row 871a is eye pixel row (1) watch.

[0532]The program current which flows into the source signal line 18 is N times (in order to explain easily, it explains as N= 10 like an old example.) of a predetermined value. It is not limited to N= 10. Of course, since predetermined values are data currents which display a picture, unless it is a white raster display etc., they are not a fixed value. It is.

[0533]In drawing 97, when a write-in pixel row is (1) pixel-row eye, Vgl voltage will be impressed to the gate signal line 17a (1), and TFT11b for a drive and TFT11c for taking in will be in an ON state. Vgh voltage is impressed to the gate signal line 17b (1). Therefore, TFT11d for switching of a pixel row (1) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it serves as the non display regions 312.

[0534]A write-in pixel row is (3) pixel-row eye the following 1H. Vgl voltage will be impressed to the gate signal line 17a (3), and TFT11b for a drive and TFT11c for taking in will be in an ON state. Vgh voltage is impressed to the gate signal line 17b (3). Therefore, TFT11d for switching of a pixel row (3) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it serves as the non display regions 312. Vgl voltage is impressed to the gate signal line 17b (1), and TFT11d for switching is an ON state. Therefore, TFT11d for switching of a pixel row (1) is also an ON state, and corresponding EL element 15 of a pixel row emits light.

[0535]A write-in pixel row is (5) pixel-row eye the following 1H. Vgl voltage is impressed to the gate signal line 17a (5), and TFT11b for a drive and TFT11c for taking in are ON states. Vgh voltage is impressed, TFT11d for switching of a pixel row (5) will be in an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the gate signal line 17b (5) with the non display regions 312. Vgl voltage is impressed to the gate signal line 17b (3), and TFT11d for switching is an ON state. Therefore, TFT11d for switching of a pixel row (3) is also an ON state, and corresponding EL element 15 of a pixel row emits light.

[0536]As mentioned above, in the 1st field, an odd number pixel row is chosen one by one, and image data is written in.

[0537]In the 2nd field, image data is written in one by one from (2) pixel-row eye. Vgl voltage will be impressed to the gate signal line 17a (2), and TFT11b for a drive and TFT11c for taking in will be in an ON state. Vgh voltage is impressed, TFT11d for switching of a pixel row (2) will be in an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the gate signal line 17b (2) with the non display regions 312.

[0538]A write-in pixel row is (4) pixel-row eye the following 1H. Vgl voltage will be impressed to the gate signal line 17a (4), and TFT11b for a drive and TFT11c for taking in will be in an ON state. Vgh voltage is impressed, TFT11d for switching of a pixel row (4) will be in an OFF state, and current does not flow into

corresponding EL element 15 of a pixel row, but it becomes the gate signal line 17b (4) with the non display regions 312. Vgl voltage is impressed to the gate signal line 17b (3), and TFT11d for switching is an ON state. Therefore, TFT11d for switching of a pixel row (3) is also an ON state, and corresponding EL element 15 of a pixel row emits light.
[0539]A write-in pixel row is (6) pixel-row eye the following 1H. Vgl voltage will be impressed to the gate signal line 17a (6), and TFT11b for a drive and TFT11c for taking in will be in an ON state. Vgh voltage is impressed, TFT11d for switching of a pixel row (6) will be in an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the gate signal line 17b (6) with the non display regions 312. Vgl voltage is impressed to the gate signal line 17b (4), and TFT11d for switching is an ON state. Therefore, TFT11d for switching of a pixel row (4) is also an ON state, and corresponding EL element 15 of a pixel row emits light.
[0540]As mentioned above, in the 2nd field, an even number pixel row is chosen one by one, and image data is written in. The image display of one sheet is completed in this 1st field and 2nd field. In the 2nd field, when writing an even number pixel row, all odd number pixel rows are made into the non display regions 312. In the 1st field, when writing an odd number pixel row, all even number pixel rows are made into the non display regions 312.
[0541]However, if 10 times as much current (N= 10) is sent through the source signal line 18 and current programming is made TFT11a for conversion with the drive method of drawing 96, even if it carries out processing in which an odd number pixel row or an even number pixel row is displayed by turns, display luminance will turn into the one 2= 5 times luminosity [10 /] of this of predetermined luminosity. Therefore, in order to make display luminance into 1 time, it is necessary to drive by N= 2. However, since the current value written in the source signal line 18 cannot fully carry out the charge and discharge of the parasitic capacitance 404 small if it drives by N= 2, writing shortage occurs to the capacitor 19 and resolution falls.
[0542]What is necessary is just to let an odd number pixel row or not only an even number pixel row but a part of display screen 21 be the non display regions 312a so that you may illustrate to drawing 98 in order to solve this. In drawing 98, it is scanned with drawing 98 (a) -> drawing 98 (b) -> drawing 98 (c) -> drawing 98 (a). A viewing area is formed in the write-in pixel row 871a upper part in the predetermined range so that it may understand by drawing 98 (b) (while scanning down from on a screen). However, since a viewing area is an odd number pixel row or an even number pixel row, it becomes every pixel row. The non display regions 312a are made into continuous non display regions.
[0543]However, like the drive method of drawing 98, if a viewing area is hardened in part to a display screen and scanned to it, it will become easy to generate a flicker. However, when a frame rate is not less than 80 Hz, cautions are taken for a flicker not to occur, even if it is a displaying condition of drawing 98 (when the image display region 311 is set to one). If a frame rate shall be not less than 80 Hz, it becomes unnecessary that is, to divide the image display region 311.
[0544]What is necessary is just to divide so that it may illustrate to drawing 99, when a frame rate is low. Probably, drawing 99 does not have **** in explanation daringly, since this was explained previously. However, drawing 99 drew as a divided field in the pair of the non display regions 312b and the image display region 311 in order to draw easily, but even if two or more non display regions 312b and two or more image display regions 311 exist in the field which it is not limited to this and divided, it is satisfactory.

[0545]Various composition can be considered to a drive system. In drawing 100, when a write-in pixel row is (1) pixel-row eye, as for the gate signal line 17a, (1) and (G) are chosen. That is, TFT11b for a drive of a pixel row (1) and (G) and TFT11c for taking in are ON states. Vgh voltage is impressed to the gate signal line 17b. Therefore, TFT11d for switching of a pixel row (1) and (G) is an OFF state at least, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.
[0546]Since the pixel rows chosen simultaneously are two pixel rows (K= 2), the TFT11a for two conversion operates. That is, 10 per pixel / 2= 5 times as many current flows into TFT11a for conversion. The current which added two program current of TFT11a for conversion flows into the source signal line 18.
[0547]After the following 1H, the gate signal line 17a (G) serves as non selection, and ON state voltage Vgl is impressed to the gate signal line 17b (G). Simultaneously, the gate signal line 17a (2) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (2). By operating in this way, regular image data is held at a pixel row (G).
[0548]After the following 1H, the gate signal line 17a (1) serves as non selection, and ON state voltage Vgl

is impressed to the gate signal line 17b (1). Simultaneously, the gate signal line 17a (3) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for conversion of the selected pixel row (3). By operating in this way, regular image data is held at a pixel row (1). One screen is rewritten by scanning, shifting one pixel row at a time with the above operation.
[0549]What is necessary is just to divide the non display regions 312 or the image display region 311 into plurality so that it may illustrate to Drawing 101 when it is easy to generate a flicker. Probably, Drawing 101 does not have **** in explanation daringly, since this was explained previously.
[0550]Drawing 102 and Drawing 103 show false interlace driving. With false interlace driving, the 1st F (the 1st field) writes in image data, without choosing simultaneously the 2-pixel (two or more pixels) line of an odd number pixel row and an even number pixel row, and the selected pixel row lapping. the [of the following] -- 2F is a method which writes in image data, without the pixel row which chose simultaneously the 2-pixel (two or more pixels) line of an even number pixel row and an odd number pixel row, and chose it lapping except for the 1st pixel row.
[0551]Drawing 103 (a1), (a2), and (a3) are the 1st field, and Drawing 103 (b1), (b2), and (b3) are the 2nd field. The 1st field writes in picture image data for the write-in pixel row 871 in 2 pixel-row pair one by one with figure 103 (a1) -> figure 103 (a2) -> figure 103 (a3) ->. Therefore, two pixel rows are identical image displays, and period maintenance of the 1 field is carried out for this displaying condition. In the 1st field, the image data of an odd number pixel row is displayed on an applicable odd number pixel row and the next even number pixel row. That is, the image data of the 1st line is displayed on the 1st pixel row and the 2nd pixel row, the image data of the 3rd line is displayed on the 3rd pixel row and the 4th pixel row, the image data of the 5th line is displayed on the 5th pixel row and the 6th pixel row, and the image data of the 7th line is displayed on the 7th pixel row and the 8th pixel row.
[0552]The 2nd field writes in picture image data for the write-in pixel row 871 in 2 pixel-row pair one by one with figure 103 (b1) -> figure 103 (b2) -> figure 103 (b3) ->. Therefore, two pixel rows are identical image displays, and period maintenance of the 1 field is carried out for this displaying condition. In the 2nd field, the image data of an even number pixel row is displayed on an applicable even number pixel row and the next odd number pixel row. That is, the image data of the 2nd line is displayed on the 2nd pixel row and the 3rd pixel row, the image data of the 4th line is displayed on the 4th pixel row and the 5th pixel row, the image data of the 6th line is displayed on the 6th pixel row and the 7th pixel row, and the image data of the 8th line is displayed on the 8th pixel row and the 9th pixel row.
[0553]As for the 1st pixel row of Drawing 103 (a1), the state of the 1st field is kept held. Although odd number image data is written in and even number image data is written in in the 2nd field, it may not be limited to this, and reverse may be sufficient in the 1st field.
[0554]When carrying out image display as mentioned above, and when the display image of the 2 fields is put together in addition, and appears by an afterimage by human being's eyes and one frame (2 field) is completed, the 1st pixel row is a display image of the 1st field. The image data of the 1st pixel row of the 1st field and the image data of the 2nd pixel row of the 2nd field were added to the 2nd pixel row. To the 3rd pixel row, the image data of the 3rd pixel row of the 1st field and the image data of the 2nd pixel row of the 2nd field were added. The image data of the 3rd pixel row of the 1st field and the image data of the 4th pixel row of the 2nd field were added to the 4th pixel row. To the 5th pixel row, the image data of the 5th pixel row of the 1st field and the image data of the 4th pixel row of the 2nd field were added.
[0555]As mentioned above, since each pixel row becomes that to which the picture of the two fields piled up and was joined, the outline of a display image becomes smooth. Although some animation dotage occurs in animation display especially, good resolution is mostly obtained with a still picture (recognized like).
[0556]Drawing 104 shows the driving waveform for realizing the method of presentation of Drawing 103. The upper position of a drawing is a driving waveform of the 1st field (1F), and the lower position of a drawing is a driving waveform of the 2nd field (2F).
[0557]In the 1st field (1F), the gate signal line 17a (1) and (2) of the 1st pixel row and the 2nd pixel row is chosen first. Since 10 times (N= 10) as much driving current flows into the source signal line 18, it is programmed with 5 times as much current by TFT11a for conversion of a pixel row (1) and (2), respectively. At this time, OFF state voltage Vgh is impressed to the gate signal line 17b (1) and (2) of the 1st pixel row and the 2nd pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 1st pixel row and the 2nd pixel row is not turned on.
[0558]The gate signal line 17a (3) and (4) of the 3rd pixel row and the 4th pixel row is chosen after 2H (since even number pixel row or odd number pixel row [every] image data is written in, set to 2H), and 10 times (N= 10) as much driving current flows into the source signal line 18. Therefore, TFT11a for conversion of a pixel row (3) and (4) is programmed with 5 times as much current, respectively. At this

time, OFF state voltage Vgh is impressed to the gate signal line 17b (3) and (4) of the 3rd pixel row and the 4th pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 3rd pixel row and the 4th pixel row is not turned on.
[0559]On the other hand, since ON state voltage Vgl is impressed to the gate signal line 17b (1) and (2), and EL element 15 turns it on. [TFT11d for switching of the 1st pixel row and the 2nd pixel row]
[0560]The gate signal line 17a (5) and (6) of the 5th pixel row and the 6th pixel row is chosen after 2H. Since 10 times (N= 10) as much driving current flows into the source signal line 18, it is programmed with 5 times as much current by TFT11a for conversion of a pixel row (5) and (6), respectively. At this time, OFF state voltage Vgh is impressed to the gate signal line 17b (5) and (6) of the 5th pixel row and the 6th pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 5th pixel row and the 6th pixel row is not turned on.
[0561]On the other hand, since ON state voltage Vgl is impressed to the gate signal line 17b (1), (2), (3), and (4), and EL element 15 lights up. [TFT11d for switching of the 1st pixel row, the 2nd pixel row, the 3rd pixel row, and the 4th pixel row] The above operation is carried out to the last odd number pixel row of a screen, and one screen is displayed.
[0562]The 1st pixel row is not chosen but makes the state of the 1st field hold in the 2nd field (2F). Next, the gate signal line 17a (2) and (3) of the 2nd pixel row and the 3rd pixel row is chosen. 10 times (N= 10) as much driving current flows into the source signal line 18. Therefore, it is programmed with 5 times as much current by TFT11a for conversion of a pixel row (2) and (3), respectively. At this time, OFF state voltage Vgh is impressed to the gate signal line 17b (2) and (3) of the 2nd pixel row and the 3rd pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 2nd pixel row and the 3rd pixel row is not turned on.
[0563]The gate signal line 17a (4) and (5) of the 4th pixel row and the 5th pixel row is chosen after 2H, and 10 times (N= 10) as much driving current flows into the source signal line 18. Therefore, it is programmed with 5 times as much current by TFT11a for conversion of a pixel row (4) and (5), respectively. At this time, OFF state voltage Vgh is impressed to the gate signal line 17b (4) and (5) of the 4th pixel row and the 5th pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 4th pixel row and the 5th pixel row is not turned on.
[0564]On the other hand, since ON state voltage Vgl is impressed to the gate signal line 17b (2) and (3), and EL element 15 is turned on. [TFT11d for switching of the 1st pixel row, the 2nd pixel row, and the 3rd pixel row]
[0565]The gate signal line 17a (6) and (7) of the 6th pixel row and the 7th pixel row is chosen after 2H, and 10 times (N= 10) as much driving current flows into the source signal line 18. Therefore, it is programmed with 5 times as much current by TFT11a for conversion of a pixel row (6) and (7), respectively. At this time, OFF state voltage Vgh is impressed to the gate signal line 17b (6) and (7) of the 6th pixel row and the 7th pixel row, and TFT11d for switching is an OFF state. Therefore, EL element 15 of the 6th pixel row and the 7th pixel row is not turned on.
[0566]On the other hand, since ON state voltage Vgl is impressed to the gate signal line 17b (1), (2), (3), (4), and (5), and EL element 15 is turned on. [TFT11d for switching of the 1st pixel row, the 2nd pixel row, the 3rd pixel row, the 4th pixel row, and the 5th pixel row] The above operation is carried out to the last even number pixel row of a screen, and one screen is displayed.
[0567]The above example displays one screen in the 2 field. Drawing 105 displays one screen in the 2 or more fields. In Drawing 105 (a), the 1st field and Drawing 105 (b) show [the 2nd field and Drawing 105 (c)] the 3rd field.
[0568]In the 1st field, Y-43 (Y is one or more integers) pixel row and Y-42 pixel row write in, and it is the pixel row 871. It writes in two pixel rows of image data at a time. In the 2nd field, Y-41 pixel row and 4Y pixel row write in, and it is the pixel row 871. It writes in two pixel rows of image data at a time for the previous field similarly. In the 3rd field, Y-42 pixel row and Y-41 pixel row write in, and it is the pixel row 871. It writes in two pixel rows of image data at a time. Each picture element data is complemented with the image data of two or more fields by writing in by 3F as mentioned above.
[0569]Although Drawing 105 showed the example of one screen in the 3 fields, image display may be realized using the field beyond it. For example, in the case of the 4 field, Y-43 (Y is one or more integers) pixel row and Y-42 pixel row write in, and it is the pixel row 871 in the 1st field. It writes in two pixel rows of image data at a time. In the 2nd field, Y-41 pixel row and 4Y pixel row write in, and it is the pixel row 871. In the 3rd field, Y-42 pixel row and Y-41 pixel row write in, and it is the pixel row 871. It writes in two pixel rows of image data at a time like the point. In the 4th field, Y-43 pixel row and 4Y pixel row write in, and it is the pixel row 871. It writes in two pixel rows of image data at a time for the previous field similarly.

Each picture element data is complemented with the image data of two or more fields by writing in as mentioned above in the 4 fields.
[0570]Although the above example mainly illustrated and explained the pixel configuration of drawing 6, its drive method of this invention is effective also to other current programming pixel configurations, such as drawing 8 and drawing 68.
[0571]Drawing 106 is an explanatory view of the drive method of the pixel configuration of drawing 68. Current sent through the source signal line 18 from the source driver 14 also here in order to explain easily (or) The current which the source driver 14 absorbs from the source signal line 18, and the current which TFT11a for a drive slushes into the source signal line 18 explain as 10 times (N= 10) of a predetermined value. The current magnification of TFT11a for a drive and TFT11b explains noting that it is 1:1 (current magnification 1).
[0572]Therefore, if the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five drives will operate. Since it is current magnification =1, the same current as TFT11a flows also into TFT11b for a drive. That is, 10 per pixel / 5= 2 twice as many current as this flows into TFT11a for a drive. Since the current programmed by TFT11a for a drive of the pixel 16 is twice the predetermined value, the current which flows into an EL element is also twice. Therefore, degradation of EL element 15 decreases as compared with the case where 10 times as much current is sent like drawing 34. Since the current which flows into the source signal line 18 on the other hand is 10 times, the charge and discharge of the same parasitic capacitance 404 as drawing 34 are possible for it. This is the same also in drawing 35.
[0573]If current magnification is 2, the current which TFT11b for a drive sends through EL element 15 will be 1 time. Therefore, predetermined current can be sent through EL element 15 so that predetermined luminosity may be obtained. That is, the drive design of a display panel with the high degree of flexibility is possible by designing current magnification (rate of a current ratio of TFT11a and TFT11b), and the current (program current) sent through the source signal line 18 in the pixel configuration of drawing 8 and drawing 68 (adjustment).
[0574]If the pixel rows chosen simultaneously are five pixel rows (K= 5), it will become what added five program current of TFT11a for a drive. For example, the current of Idx10 will be sent through the source signal line 18, if the current to write in is originally set to Id and it is referred to as N= 10 at the write-in pixel row 871a. The write-in pixel row 871b (871b is a pixel row used auxiliary in order to make the current amount to the source signal line 18 increase.) which adjoined the write-in pixel row 871a Therefore, the pixel (line) which writes in a picture is 871a, and in order to write in 871a, it is the pixel (line) 871b which is used auxiliary.
[0575]In Drawing 106, K lines (K= 5) are simultaneously written in by the image data of the write-in pixel row 871a. Therefore, the range of K line (871a, 871b) serves as the same display. Thus, if the same display is used, resolution will fall with a natural thing. In order to cope with this, it writes in so that it may illustrate to drawing 35 (b), and let the portion of the pixel row 871b be the non display regions 312. Therefore, resolution lowering is not generated.
[0576]Since this pixel is under program, although the write-in pixel row 871a illustrated to Drawing 106 (a) is made into the displaying condition, it changes by the current writing state to a pixel. Therefore, it is good also as the non display regions 312.
[0577]After the following 1H writes in the pixel row which carried out 1 pixel-row shift, and performs the same operation as the pixel row 871a. The 1-pixel (line) shift also of the non display regions 312 is carried out. As mentioned above, the write-in pixel row 871b in which different current data from an original indicative data was written is not displayed, but if it shifts the above-mentioned operation of one line at a time, perfect image display is realizable. The charge and discharge of the parasitic capacitance 404 are also realizable within 1H period enough by the effect of the write-in pixel row 871b of using auxiliary.
[0578]Drawing 107 is an explanatory view of the driving waveform for realizing the drive method of Drawing 106. A voltage waveform sets OFF state voltage to Vgh (H level), and is setting ON state voltage to Vgl (L level). The number of the chosen pixel row is indicated in the lower berth of Drawing 107. (1), (2), (3) in a figure ... (11) shows the chosen pixel row number. The number of pixel rows is 480 by the VGA panel, and it is 768 by the XGA panel.
[0579]In Drawing 107, the gate signal line 17a (1) and the gate signal line 17b (1) are chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for a drive of the selected pixel row. The program current which flows into the source signal line 18 is N times (in order to explain easily, it explains as N= 10.) of a predetermined value. Of course, since predetermined values are data currents which display a picture, unless it is a white raster display etc., they are not a fixed value. It is. It explains by making five pixel rows into simultaneous selection (K= 5). Therefore, ideally, it is

programmed by the capacitor 19 of one pixel so that twice as many current as this flows into TFT11a for a drive.

[0580]Fundamentally, since the gate signal lines 17a and 17b are the same phases, communalizing is possible. However, it is better to separate the gate signal line 17a and the gate signal line 17b, since being controlled is preferred strictly so that TFT11d for switching may turn off and then TFT11c for taking in may turn off first when making a pixel row into selection and non selection.

[0581]When a write-in pixel row is (1) pixel-row eye, as Drawing 107 illustrated, ON state voltage Vgl is impressed to the gate signal lines 17a and 17b. Therefore, a pixel row (1), (2), (3), (4), and (5) are chosen. That is, TFT11c for taking in of a pixel row (1), (2), (3), (4), and (5) and TFT11d for switching are ON states. The gate signal line 17b serves as an opposite phase of the gate signal line 17b. Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312.

[0582]Ideally, TFT11a for a 5-pixel drive sends the current of Idx2 through the source signal line 18, respectively, and twice as many current as this is programmed by the capacitor 19 of each pixel 16. Here, in order to understand easily, it explains noting that the characteristic (Vt, S value) of each TFT11a for a drive corresponds.

[0583]Since the pixel rows chosen simultaneously are five pixel rows (K= 5), the TFT11a for five drives operates. That is, 10 per pixel / 5= 2 twice as many current as this flows into TFT11a for a drive. The current which added five program current of TFT11a for a drive flows into the source signal line 18. For example, the current originally written in the write-in pixel row 871a is set to Id, and the current of Idx10 is sent through the source signal line 18.

[0584]The four write-in pixel rows 871b which write in image data henceforth from a write-in pixel row (1) are pixel rows used auxiliary in order to make the current amount to the source signal line 18 increase. However, since behind regular image data is written in, a problem does not have the write-in pixel row 871b. Therefore, the write-in pixel row 871b is the same display as the write-in pixel row 871a between 1H periods. Therefore, let at least the write-in pixel row 871b chosen in order to make current increase be the non display regions 312.

[0585]After the following 1H, (the position of the pixel row number 6), the gate signal line 17a (1), and 17b (1) become non selection, and the data written in a pixel is become final and conclusive. Simultaneously, the gate signal line 17a (6) is chosen (position of the pixel number 2), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for a drive of the selected pixel row (6). By operating in this way, regular image data is held at a pixel row (1).

[0586]After the following 1H, the gate signal line 17a (2) and 17b (2) become non selection. The gate signal line 17a (7) is chosen (Vgl voltage), and program current flows into the source signal line 18 toward the source driver 14 from TFT11a for a drive of the selected pixel row (7). By operating in this way, regular image data is held at a pixel row (2). One screen is rewritten by scanning, shifting one pixel row at a time with the above operation.

[0587]Although it is the same as that of drawing 73, in order to program with twice as many current (voltage) as this to each pixel, by the drive method of drawing 82, the light emitting luminance of EL element 15 of each pixel will be twice ideally. Therefore, the luminosity of a display screen will be twice rather than a predetermined value.

[0588]What is necessary is just to let one half of the ranges of the display screen 21 be the non display regions 312, including the write-in pixel row 871 so that you may illustrate to drawing 34 in order to make this into predetermined luminosity. Since it explained using drawing 79 etc., this is omitted. It cannot be overemphasized that the drive method of drawing 89 is also applicable to drawing 68, drawing 70, drawing 75, drawing 76, Drawing 106, etc. Since explanation is given previously, it omits.

[0589]Although drawing 34 and drawing 35 illustrated and explained the pixel configuration of drawing 6, drawing 8, and a current programming method like drawing 68, it is not limited to this. For example, the pixel configuration of voltage program methods, such as drawing 70, drawing 75, and drawing 76, is also effective. Since preliminary charging of the pixel can be carried out by considering it as the method which impresses voltage to two or more pixel line simultaneously, it can respond also to the high definition display panel more than SXGA. It is because ********** and a digital disposal circuit are simplified and a good black display can be realized.

[0590]It explains by illustrating the pixel configuration of drawing 70 as an example of application of a voltage program. Drawing 108 and Drawing 109 show the driving waveform. It explains noting that five pixel rows are made into the non display regions 312 in Drawing 108 and Drawing 109, but it is for not being limited to this and only explaining easily. For example, simultaneous selection of the two pixel rows may be

made, and ten pixel rows may be sufficient. It is good also considering one pixel row as the non display regions 312. This is the same also to drawing 74, drawing 75, drawing 76, etc.
[0591]The drive method explained with drawing 86, drawing 89, drawing 93, drawing 94, drawing 96, Drawing 105, etc. is applicable to the pixel configuration of the voltage program illustrated by drawing 70, drawing 74, drawing 75, drawing 76, etc. It cannot be overemphasized that the drive method of driving so that N times as much current may flow into EL element 15, and forming the non display regions 312 is also applicable. However, with Drawing 108 and Drawing 109, since explanation becomes complicated, it does not dare to explain.
[0592]As shown in Drawing 109, when a write-in pixel row is (1) pixel-row eye (position of the pixel row number 5), as for the gate signal line 17a, (1), (2), (3), (4), and (5) are chosen. That is, TFT11b for a drive of a pixel row (1), (2), (3), (4), and (5) is an ON state, and OFF state voltage Vgh is impressed to the gate signal line 17b. Therefore, TFT11d for switching of a pixel row (1), (2), (3), (4), and (5) is an OFF state, and current does not flow into corresponding EL element 15 of a pixel row, but it becomes the non display regions 312. Therefore, preliminary charging of the voltage will be carried out to the pixel row (1) during 5H.

[0593]The pixel row by which preliminary charging is carried out is the display same between 5H periods as other four pixel rows. Therefore, let at least the pixel row which is writing in be the non display regions 312. Since picture image data approximates especially in the pixel which adjoined in the video signal, if preliminary charging is performed, the writing of regular image data will become easy.
[0594]Therefore, this invention is the method of making it into the non display regions 312 until it writes image data in two or more pixel rows and regular image data is written in. However, since the display is unstable while writing in the image data of this pixel row even if it is selection of one pixel row, it is also a concept of this invention to suppose that it is non-display. The current which flows into EL element 15 is made larger than a predetermined value, and it is made predetermined luminosity by forming the non display regions 312. The effect of this invention also realizes a good animation with this method of presentation.
[0595]The image data of (2) pixel-row eye is made to become final and conclusive in the following 1H. With Drawing 109, OFF state voltage is impressed to the gate signal line 17a (1) and the gate signal line 17b (1) so that clearly (pixel row number 6). (since Vgl:TFT 11b is N channel) ON state voltage is impressed to the gate signal line 17a (6) and the gate signal line 17b (6) (since Vgh:TFT 11b is N channel). Therefore, the image data to TFT11a for conversion of a pixel row (2) is held.
[0596]One screen can be displayed by one pixel row and a write-in pixel row shifting, and carrying out the above-mentioned operation one by one as mentioned above, synchronizing with a horizontal scanning period.
[0597]Drawing 108 shows the shifted method 1H about the timing of the gate signal line 17b in the pixel configuration of drawing 70. With Drawing 108, the pixel to become final and conclusive is made into a displaying condition so that clearly.
[0598]For example, image data is written during 5H in the pixel row (1) (period of the pixel row numbers 1-5). That is, the gate signal line 17a of a pixel row (1) is a selective state (since TFT11b is N channel, ON state voltage Vgh is impressed). Since ON state voltage is impressed to the gate signal line 17b (1) at the time of 5H (since Vgl:TFT 11d is P channel), current is flowing into EL element 15. Therefore, EL element 15 is a lighted condition. This point differs from Drawing 109. Although it was considered as the non display regions 312 in Drawing 109, since it is the same as that of Drawing 109 in respect of others, explanation is omitted.
[0599]In the example of this invention which makes one simultaneously two or more above pixel rows, and writes in image data, the pixel row of the uppermost side of the display screen 21, the lowest neighborhood, or its both does not have the pixel row adjoined for making it one simultaneously. What is necessary is just to form or arrange a dummy pixel row to this technical problem to the uppermost side of the display screen 21, the lowest neighborhood, or its both.
[0600]For example, four pixel rows are formed in the lower side of a screen in the drive method which chooses simultaneously five pixel rows explained by drawing 81. When carrying out a flip vertical drive, of course, four straw-man pixel rows are provided also in the top chord of a screen. Since this straw-man pixel row does not form EL element 15, luminescence is not carried out. Of course, even if it forms EL element 15, it is made not to emit light, or it shades and is made not to be displayed. In addition, in drawing 6, it may form except 1-pixel TFT11d for switching. One or more pixel rows of straw-man pixel rows are formed.
[0601]Although the pixel row which adjoined was carried out to making it one simultaneously, it is not limited to this. For example, the timing which makes two or more pixel rows one may differ. The effect is

demonstrated even if separated from the 1st line like two pixel rows of the 3rd line. When choosing two pixel rows, one pixel row is made one [fix and] (for example, the bottom pixel row or straw-man pixel row of a screen), and other one pixel rows may be scanned and it may be made one [extremely] one by one.
[0602]Although it is a matter common to current programming methods, such as drawing 6, drawing 8, drawing 51, drawing 61, drawing 62, and drawing 63, there is a problem that a black display with a current programming method is difficult (it is substantially improvable if this inventions, such as drawing 34 and drawing 35, are carried out, of course.). However, combining with the following examples further is also effective. Of course, it may not combine with the example of drawing 34 and drawing 35, but the following examples may be carried out independently. for example, even if the white peak current sent through EL element 15 is 2microA, it can set to 64 gradation displays -- eyes are 2microA/64**30nA 1 gradation. It is rather difficult to carry out the charge and discharge of the parasitic capacitance 404, such as the source signal line 18, to 1H period with this minute current. Although the pixel 16 is formed or arranged at matrix form, in order to explain easily, only 1 pixel is illustrated in the drawing.
[0603]In order to cope with this technical problem, in this invention, the voltage source 401 for writing the voltage (current) of a black level in the source signal line 18 is formed or arranged. In the voltage source 401, prescribed voltage is generated by a DCDC converter, and specifically, it constitutes so that this voltage can be impressed by the power supply switching means 403 which comprises an analog switch etc.
[0604]The example of the signal wave form impressed to the source signal line 18 is shown in Drawing 110. OFF or the voltage Vb mostly made a black display is impressed to the source signal line 18 of TFT11b for a drive (drawing 6 TFT11a for conversion) during [of the beginning of 1H period which performs current programming] t2. It generates in the voltage source 401 and this voltage is impressed to the source signal line 18 by the power supply switching means 403. In a program period, since TFT11c for taking in and TFT11d for switching are ON states, the voltage Vb impressed to the source signal line 18 turns into the terminal voltage of the capacitor 19, i.e., the gate terminal voltage of TFT11b for a drive. Therefore, the pixel of the beginning of 1H period serves as a black display (astigmatism light state).
[0605]Originally, when the picture displayed is a black display, the terminal voltage of the capacitor 19 is held as it is. In the case where the picture actually displayed is a white display, the voltage Vw (in addition, in the case of current programming, it should be expressed as Iw) of a white display is impressed after Vb voltage impressing, this voltage (current) is held at the capacitor 19, and 1H period expires. In order to explain easily here, since the picture actually displayed was a white display, it was presupposed that the voltage Vw (current Iw) of a white display is impressed. However, the voltage on which it is held with a natural thing at the capacitor 19 in the case of natural drawing is the voltage (current) between Vw(s) from Vb.
[0606]By impressing a signal to the source signal line 18, and driving the gate signal lines 17a and 17b, a good black display can be realized and image display, such as drawing 38, can be carried out so that it may illustrate to Drawing 110.
[0607]When the pixel configuration of drawing 6 also impresses the signal wave form of Drawing 110, a good black display is realizable. OFF or the voltage Vb mostly made a black display is impressed to the source signal line 18 of TFT11a for conversion during [of the beginning of 1H period which performs current programming] t2. It generates in the voltage source 401 and this voltage is impressed to the source signal line 18 by the power supply switching means 403.
[0608]In a program period, since TFT11b for a drive and TFT11c for taking in are ON states, the voltage Vb impressed to the source signal line 18 turns into the terminal voltage of the capacitor 19, i.e., the gate terminal voltage of TFT11a for conversion. Therefore, the pixel of the beginning of 1H period serves as a black display (astigmatism light state).
[0609]As explained previously, in the case where the picture displayed is a black display, the terminal voltage of the capacitor 19 is held as it is. In the case where the picture actually displayed is a white display, the voltage Vw (in addition, in the case of current programming, it should be expressed as Iw) of a white display is impressed after Vb voltage impressing, this voltage (current) is held at the capacitor 19, and 1H period expires.
[0610]The voltage source 401 (precharge circuit) illustrated by drawing 51 etc. is low-temperature-polysilicon art etc., and may be directly formed on the array substrate 49. Since EL element 15 differs [B / R, G, and] in element composition and material, it differs in the voltage (current) which generating of light produces in many cases (rise voltage (current)). As for one color, in order to correspond to this characteristic, it is preferred constituting so that precharge voltage can be individually set up by R, G, and B, and among at least the three primary colors to enable it to change.
[0611]It is necessary to make into 1 microseconds or more precharge time t2 which impresses Vb voltage.

As for the precharge time t2 which impresses Vb voltage, it is preferred to make it to 8% or less not less than 2 more% 10% or less more than per % of 1H.
[0612]It is preferred to constitute from contents (a luminosity, a definition, etc.) of the display screen 21 so that the voltage to precharge can be changed. For example, by pushing an adjustment switch or turning adjustment BORIUMU, a user detects this change and changes the value of precharge voltage (current). It may constitute so that it may be made to change with the contents of the picture to display, and data automatically. For example, photosensor detects the strength of external outdoor daylight and precharge (discharge) voltage (current) is adjusted with the detected value. In addition, precharge (discharge) voltage (current) is adjusted according to the kinds (a personal computer picture, the screen of daytime, a starlit sky, etc.) of picture. It opts for adjustment in consideration of the average luminosity of a picture, maximum luminance, minimum luminance, an animation, a still picture, and luminance distribution.
[0613]Drawing 51 explained the precharge circuit etc. simply. It explains in more detail using Drawing 111 etc. Since discharge and precharge are only the applying directions of potential, they make discharge and precharge homonymy and explain them henceforth using precharge.
[0614]Drawing 111 shows the circuitry which combined the current drive and the voltage drive. It is connected to the source signal line 18 with a viewing area, and the switching circuit 1223 comprises an analog switch. Voltage is impressed to a terminal of the switching circuit 1223 (precharge voltage), and the program current programmed to a pixel is impressed to b terminal.
[0615]8 bits (256 gradation) IDATA is inputted into the current output circuit 1222, the DA translation of this IDATA is carried out in the DA circuit 1226, and it serves as analog voltage. This analog voltage is impressed to the base terminal of the output transistor (or FET) 1227, and is changed into a current output in an operation of the operational amplifier 1224b and the resistance 1228. The voltage-current conversion circuit by the output transistor 1227, the operational amplifier 1224, etc. is common, and probably, the explanation beyond this does not have ****, since it is publicly known for the engineer of the technical field concerned.
[0616]On the other hand, the voltage output circuit 1221 comprises a buffer circuit by adjustment BORIUMU (VR) 1225 and the operational amplifier 1224a. Adjustment BORIUMU 1225 is common to all the source signal lines. The precharge voltage Vb is determined by adjusting this adjustment BORIUMU 1225.
[0617]When the precharge voltage Vb of the beginning of one horizontal scanning period (1H) is impressed, the switching circuit 1223 connected to all the source signal lines is connected with the terminal a. Therefore, all the source signal lines 18 are set as the precharge voltage Vb. Then, the switching circuit 1223 is changed to the terminal b, and the current data (256 gradation) corresponding to a picture is impressed to the source signal line 18. This current data is written in each pixel 16, and current flows and emits light to EL element 15 of each pixel.
[0618]Although the precharge voltage Vb was a fixed value in Drawing 111, it is the circuitry figure which enabled it to take precharge voltage 256 values (8 bits) in Drawing 112. In Drawing 112, 8-bit VDATA is inputted and the voltage output circuit 1221 is changed into analog voltage in the DA circuit 1226a. The changed analog voltage is inputted into one terminal of the operational amplifier 1224c, and it is constituted so that it can adjust to predetermined voltage to the reference voltage of adjustment BORIUMU (VR) 1225.

[0619]The output of the operational amplifier 1224c is impressed to a terminal of the switching circuit 1223a via the operational amplifier 1224a of a buffer. On the other hand, the current output is impressed to b terminal of the switching circuit 1223a.
[0620]VDATA is the voltage corresponding to IDATA. The precharge voltage Vb corresponding to VDATA is impressed to 1-10micro sec (it is preferred that it is or more 1/100 1/5 or less period of 1H) of the period of the beginning of one horizontal scanning period (1H). At this time, the switching circuit 1223 connected to all the source signal lines is connected with the terminal a. Therefore, each source signal line 18 is set as the precharge voltage Vb corresponding to VDATA. The difference with Drawing 111 is being able to set the precharge voltage Vb as each source signal line. That is, DA circuit which carries out the DA translation of the IDATA to each source signal line 18, respectively, and DA circuit which carries out the DA translation of the VDATA are provided. However, it is not limited to providing DA circuit which carries out the DA translation of the IDATA to each source signal line 18, respectively, and DA circuit which carries out the DA translation of the VDATA. For example, it is because DA circuit is realizable at least one if sample hold of the output is carried out with each source signal line.
[0621]Although the voltage which changed VDATA is impressed to the period of the beginning of 1H, this pressure value becomes almost equal to the source signal line potential by the current value corresponding to IDATA impressed henceforth. Therefore, by impressing the voltage of VDATA, the potential of a source

signal line serves as a desired value mostly, and is amending to a desired value slightly by IDATA. By constituting as mentioned above, the current writing shortage to the source signal line 18 is lost.
[0622]In Drawing 112 (a), although the switching circuit 1223a presupposed that a terminal and b terminal are changed, it is not limited to this. For example, as shown in Drawing 112 (b), the output of the voltage output circuit 1221 may be impressed to a terminal, and it may constitute so that the output of the current output circuit 1222 may be to the source signal line 18 in a connected state continuously.
[0623]The pliability of circuitry improves further by the ability to carry out the output change of the DA circuit 1226 corresponding to reference voltage. That an output change can be carried out corresponding to this reference voltage means what can change an output at 0.01V interval, when reference voltage is 2.54V (when DA circuit of 8 bits and 256 gradation is adopted). Reference voltage can change an output at 0.02V interval 5.08V. That is, the output of DA circuit can be changed in proportion to reference voltage in an instant by changing reference voltage. Drawing 113 is a circuit block figure at the time of adopting such a DA circuit.
[0624]In Drawing 113, Vref voltage is impressed to the DA circuit 1226a. Vref voltage is outputted from the circuit which consists of RV* resistance which quadrisects Vv voltage, and the switching circuit 1223b. Therefore, Vref voltage is changed to four steps by a CVS signal, and can change the output of the DA circuit 1226a in an instant in four steps.
[0625]On the other hand, Iref voltage is impressed to the DA circuit 1226b. Iref voltage is outputted from the circuit which consists of RV* resistance which quadrisects Vi voltage, and the switching circuit 1223c. Therefore, Iref voltage is changed to four steps by a CIS signal, and can change the output of the DA circuit 1226b in an instant in four steps.
[0626]By constituting, as shown in Drawing 113, the current (voltage) outputted to the source signal line 18 can change now to four steps during 1H. As these directions for use, high voltage (current) can be impressed first for a moment, and it can be made to be able to reach to a desired value at high speed by this impression, and can change into the voltage (current) of a steady-state value after that, and the voltage (current) written in a pixel can be changed at high speed by using a desired value.
[0627]However, in the composition of Drawing 113, circuit structure will become quite big. The composition generally illustrated to Drawing 114 is enough. The composition of Drawing 113 is constituted so that the voltage output circuit 1221 can output two pressure values. These two voltage is voltage to which one makes image display black. Other one is voltage which makes image display white. If Vdd voltage of drawing 6 is set to 6V, black voltage will be 3V-4V, and, specifically, white voltages will be 1V-2V. This white voltage and black voltage are adjusted by adjustment BORIUMU (VR) 1225, and this voltage is impressed to the switching circuit 1223b via the operational amplifiers 1224a and 1224c of a buffer. The output of the switching circuit 1223b is changed on VSL voltage.
[0628]The precharge voltage Vb (white voltage or black voltage) is impressed to the beginning of one horizontal scanning period (1H). Since each source signal line is connected with the terminal c of the switching circuit 1223a, precharge setting out of each source signal line 18 is carried out first at white voltage or black voltage. Then, the switching circuit 1223 is changed to the terminal b, and the current data (256 gradation) corresponding to a picture is impressed to the source signal line 18. This current data is written in each pixel 16, and current flows and emits light to EL element 15 of each pixel.
[0629]In the above example, although each source signal line 18 presupposed first that it is set as precharge at white voltage or black voltage, it is not limited to this. It is more realistic to constitute so that it may precharge when an indicative data (VDATA, IDATA) is beyond a predetermined value, or when it is below a predetermined value.
[0630]Drawing 115 has illustrated the case of 64 gradation displays in order to illustrate easily. In Drawing 115 (a), the range of eyes (kW) is precharged with white voltage 63 gradation from eyes 57 gradation. That is, white voltage is outputted from the voltage output circuit 1221 of Drawing 114. The range of eyes (KB) is precharged on black voltage 7 gradation from eyes 0 gradation. That is, black voltage is outputted from the voltage output circuit 1221 of Drawing 114. And eyes make the output of the voltage output circuit 1221 a high impedance state 56 gradation from eyes 8 gradation (the switching circuit 1223a does not choose the terminal a).
[0631]As mentioned above, white voltage is impressed to the gradation which should be considered as a white display, and black voltage is impressed to the gradation which should be considered as a black display. A gradation display is realizable at high speed and good by not precharging in the part (KM) of intermediate color.
[0632]In the case of a current programming method, in a black display, since program current (current written in a pixel) is as small as 20 or less nA of 5 or more nA, writing shortage occurs. Then, an original

black display is realizable by precharging black voltage. However, writing shortage may also generate a dark gray display. In this case, it is effective to perform 2nd black precharge in addition to white and black precharge.

[0633]Drawing 115 (b) shows this example. By precharging black voltage in KB1, an original black display is realizable. And sufficient gradation display is realizable to the gray portion near black by precharging the 2nd black (gray) for the range of KB2.

[0634]Here, if Vdd voltage sets to 6V in the pixel configuration of drawing 6, more specifically, the black voltage which the black voltage which precharges the range of KB1 is 3V-3.5V, and performs gray precharge of KB2 will be 3.5V-4.0V. The white voltages of the range of KW are 1V-2V. The precharge by voltage does not perform the range of KM.

[0635]Drawing 115 (b) has illustrated the case of 64 gradation displays in order to illustrate easily. In Drawing 115 (b), the range of eyes (kW) is precharged with white voltage 63 gradation from eyes 57 gradation. The range of eyes (KB1) is precharged on black voltage 7 gradation from eyes 0 gradation. The range of eyes (KB2) is precharged on the 2nd black voltage 15 gradation from eyes 8 gradation. Eyes make the output of the voltage output circuit 1221 a high impedance state 56 gradation from eyes 16 gradation (the switching circuit 1223a does not choose the terminal a).

[0636]As mentioned above, the black range is divided into two or more ranges, and a more proper gradation display can be realized by precharging on voltage different, respectively. Although Drawing 115 (b) is made into two black ranges, it may not be limited to this, and three or more may be sufficient as it. Precharge may be put in block to all the source signal lines, and may be performed. Since what is necessary is just to constitute these circuitry so that the three or more operational amplifiers 1224 of a buffer may be arranged in Drawing 114 and the three or more switching circuits 1223b can be chosen, it is easy.

[0637]In Drawing 115, the current sent through the gradation 0 (black display) at EL element 15 is not 0A. EL element 15 does not emit light, unless it sends beyond predetermined current. The current of this range that does not emit light is called dark current. Dark current is about 50 or less nA in pixel size of 10 or more nA in 10000 square mum. A pixel is a black display and current is flowing through it within the limits of this dark current also with the gradation 0. It is necessary to drive with the current which added dark current as composition of the source driver 14.

[0638]Henceforth, the circuitry illustrated to Drawing 111 - Drawing 114 is called the output stage circuit 1271. The output stage circuit 1271 is an example of composition with common arranging to each source signal line 18 (formation), as illustrated to Drawing 116. With Drawing 116 etc., the output stage circuit 1271 is illustrated as formed in the source driver 14 formed with the silicon chip, but it is not limited to this, and may be directly formed simultaneously with pixel TFT11 etc. on the glass substrate 241. That is, the CGS (Continuous Grain Silicon) art which elevated-temperature polysilicon technology, low-temperature-polysilicon art, and Sharp are developing, The output stage circuit 1271 may be formed with the art which forms in a glass substrate etc. the semiconductor circuit formed in the quartz substrate in which the method and SEIKO EPSON which form in a substrate and are grown up are developing the seed crystal which FUJITSU, LTD. is developing by transfer. When the glass substrate 241 is a metal substrate or a semiconductor substrate, it cannot be overemphasized that the output stage circuit 1271 can be formed directly.

[0639]The projection electrode (not shown) which uses plating art or nail-head-bonding art for the signal terminal polar zone of said source driver, and becomes the source driver 14 from gold (Au) several to 100 micrometers high is formed. Said projection electrode and each signal wire are electrically connected via the conductive joining layer (not shown). The adhesives of a conductive joining layer are the thing which used an epoxy system, a phenol system, etc. as base resin and with which flakes, such as silver (Ag), gold (Au), nickel (nickel), carbon (C), and tin oxide (SnO_2), were mixed, or ultraviolet curing resin. This conductive joining layer is formed on a projection electrode with art, such as transfer.

[0640]Although it illustrated or explained that the source driver 14 (or gate driver 12) was loaded on a substrate, it is not limited to this. It may connect with a signal wire using the polyimide film etc. which did not load the source driver 14 (or gate driver 12) on the substrate, but loaded the driver IC using film carrier art.

[0641]Drawing 116 was illustrated as the output stage circuit 1271 had been arranged only at the end of one side of the display screen 21, but it is not limited to this. For example, the source drivers 14a and 14b may be arranged so that it may illustrate to Drawing 117. The two gate drivers 12 are also formed in Drawing 117. That is, if a display screen will comprise 21a and 21b and is constituted in this way, it can display a separate picture by the display screens 21a and 21b.

[0642]Since the display screen 21 is divided into two with the composition of Drawing 117, as compared

with the case where the number of the display screens 21 is one, one half of clock frequency may be sufficient as the video signal outputted from the output stage circuit 1271. The parasitic capacitance generated in the source signal line 18 etc. is also set to one half. Therefore, the burden of the output stage circuit 1271 is set to 1/2x1/2=1/4. Therefore, even if the current outputted from the output stage circuit 1271 is minute, the charge and discharge of the parasitic capacitance of the source signal line 17 can be carried out enough, and writing shortage does not occur.

[0643]With the composition of Drawing 117, since the display screen 21 is divided into two in the center section on Screen 21a and Screen 21b, a boundary line may be seen in a dividing position. Drawing 118 copes with this technical problem. The source driver 14a drives the odd number pixel row of the display screen 21, and the source driver 14b drives the even number pixel row of the display screen 21. Therefore, the boundary line of the display screen 21 does not occur.

[0644]In order to improve the shortage of write current to a pixel, it is good to consider the output stage circuit 1271 corresponding to each source signal line 18 as two outputs in the source drivers 14a and 14b so that it may illustrate to Drawing 119. That is, in the output stage circuit 1271a, two output stages (the output stage A, the output stage B) are provided, the output stage A is connected to the odd number pixel row of the display screen 21a, and the output stage B is connected to the even number pixel row of the display screen 21a. Two output stages (the output stage A, the output stage B) are provided also in the output stage circuit 1271b, the output stage A is connected to the odd number pixel row of the display screen 21b, and the output stage B is connected to the even number pixel row of the display screen 21b. By constituting in this way, it leads to the ability of still more sufficient current for a source signal line also by micro current to be sent, and good image display can be realized.

[0645]It is not what is limited to this although the output stage circuit 1271 presupposed that the one source signal line 18 is connected to each pixel in Drawing 119, A pixel may be made differential composition, and it may constitute so that it may drive to each pixel with two source signal lines (it is an object for bias current + signal current about the source signal line of the object for bias current, and another side in one source signal line).

[0646]Drawing 120 is a more concrete module block diagram. In Drawing 120, 14b is a source driver and 14c is the chip (1 chip driver IC) with which the gate driver and the source driver were unified. 1 chip driver IC14c is driving the gate signal line of the display screen 21. 1 chip driver IC14c drives the source signal line 18a of the display screen 21a. The source driver 14b drives the source signal line 18b, and drives display ****** 21b.

[0647]Drawing 120 shows an example, the source driver 14b also has a gate driver function, and it may constitute it so that the gate signal line 17b of the display screen 21b may be driven. Power supply IC102 and control IC101 are illustrated as loaded on the printed circuit board 103, but they are not limited to this, and may be directly formed in the display panel 82 using the polysilicon technology etc. which were explained previously. This is applicable also to Drawing 194 and Drawing 195. Since other composition is the same as that of drawing 15, Drawing 119, Drawing 194, Drawing 195, etc., explanation is omitted.

[0648]Control IC101 drives both 1 chip driver IC14c and the source driver 14b. The signals (power supply wiring, data wiring, etc.) supplied to control IC101 to 1 chip driver IC14c are supplied via the flexible substrate 104c. However, since it is considerably separated from the source driver 14b of distance, it is first connected to the rear face of the display panel 82 by the flexible substrate 104a.

[0649]Drawing 121 is a figure which observed the display panel 82 from the rear face. The signal wiring (power supply wiring is included) 1321 is formed in the rear face of the display panel 82. The signal wiring 1321 is formed with metallic materials, such as copper, aluminum (aluminum), silver, and silver-palladium, palladium, gold, and aluminum-Mo. The signal wiring 1321 transmits a signal from one end of the display panel 82 to the other. The flexible substrate 104b is connected to the end of the display panel 82, and a signal etc. are supplied to the source driver 14b from this flexible substrate 104b. Drawing 122 shows a drawing when it sees from A of Drawing 121.

[0650]Although drawing 51, Drawing 110 - Drawing 115 illustrated and illustrated the pixel configuration of drawing 6 and a current programming method like drawing 8, they are not limited to this. For example, the pixel configuration of voltage program methods, such as drawing 74, drawing 75, drawing 76, Drawing 123, and Drawing 124, is also effective. In that case, it is necessary to make into voltage the signal impressed to b terminal of the switching circuit 1223 of Drawing 111. This change is easy, and if it is human being of the technical field concerned, it will be able to respond easily. the insufficient charging according to the parasitic capacitance of the source signal line 18 by voltage drive -- ********** -- although -- it is because a drive circuit and a digital disposal circuit are simplified and a good black display can be realized by considering it as the method which impresses voltage to two or more pixel line simultaneously. It is

because the **** display of a picture can be realized and an effect is demonstrated by dispersion absorption of TFT11.
[0651]Therefore, it cannot be overemphasized that the matter explained with Drawing 111 - Drawing 115 is applicable to all the display panels of this invention, a display, an information display device, etc.
[0652]As mentioned above, this invention is applicable to various pixel configurations. Drawing 125 shows the example which used P channel of TFT11 of drawing 6 as N channel. Also in Drawing 125, TFT11d for switching can be turned on and off by controlling the gate signal line 17, and since it is needless to say, that image display, such as drawing 38, is realizable omits explanation. Since driving waveforms, such as drawing 37 and drawing 44, are also the same or similar, explanation is omitted. It is also effective to use only TFT11b for a drive and TFT11c for taking in as the N channel TFT in drawing 6. this -- the capacitor 19 -- it is because it runs, voltage falls and the holding property of a capacitor is also improved.
[0653]Drawing 125 shows the composition of providing only the current source 402. That is, the voltage source 401 which precharges is not provided. However, comparatively small [the parasitic capacitance 404], when 1H period is long enough, even if there is no voltage source 401, a black display can fully be realized. As drawing 38 etc. explained, to carry out the perfect non display regions 312, the voltage source 401 is not required in most cases. What is necessary is just to constitute so that it may illustrate to Drawing 126, when required.
[0654]Drawing 127 shows the example which used P channel of TFT11 of drawing 8 as N channel. Also in Drawing 127, TFT11e etc. can be turned on and off by controlling the gate signal line 17, and since it is needless to say, that image display, such as drawing 38, is realizable omits explanation. Since driving waveforms, such as drawing 37 and drawing 44, are also the same or similar, explanation is omitted.
[0655]As explained above, a good black display is realizable by impressing Vb voltage (Ib current) by the voltage source 401.
[0656]If N= 10 or more are used and a high current pulse is impressed to EL element 15, EL terminal voltage will also become high. EL element 15 differs [B / R, G, and] in rise voltage and a gamma curve. Since the gamma curve is loose, especially B is in the tendency for the terminal voltage of EL element 15 to become high. Rise voltage is high, and power consumption will become large if a gamma curve unites terminal voltage with EL element 15 of a loose color (R, G, B color).
[0657]One of the methods of solving this is a method which separates the cathode shown in drawing 25 by R, G, and B. It is not necessary to make it respectively different cathode potential by R, G, and B. In particular, a gamma curve may separate only the cathode of only one color which is separated from other colors. The composition which separates Vdd power supply voltage as the other methods as shown in Drawing 128 is also effective. That is, it is the composition which sets the Vdd power supply of R color to VddR, sets the Vdd power supply of G color to VddG, and sets the Vdd power supply of B color to VddB. By dissociating in this way, each RGB can be adjusted with another power supply, and even if the terminal voltage of EL element 15 of RGB differs, the increase in power consumption becomes small.
[0658]It is not necessary to make it respectively different Vdd potential by R, G, and B. In particular, a gamma curve may separate only Vdd of only one color which is separated from other colors. It may combine with the composition of drawing 25 so that it may illustrate to Drawing 129. That is, it is considered as respectively different cathode potential (as for VsR and G pixel, in R pixel, VsG and B pixel are VsB(s)) by R, G, and B which are the methods separated by R, G, and B. In particular, a gamma curve may separate only the cathode potential of only one color which is separated from other colors. Vdd power supply voltage is separated. It is the composition which sets the Vdd power supply of R color to VddR, sets the Vdd power supply of G color to VddG, and sets the Vdd power supply of B color to VddB. It is not necessary to make it respectively different Vdd potential by R, G, and B also in this case. In particular, a gamma curve may separate only Vdd of only one color which is separated from other colors.
[0659]Although the pixel 16 was considered as the composition of drawing 6 in Drawing 128 and Drawing 129, it is not limited to this and it cannot be overemphasized that the composition of drawing 8, drawing 9, drawing 56, drawing 61 - drawing 65, drawing 68 - drawing 72, drawing 74, drawing 75, Drawing 125 - Drawing 127, Drawing 130, etc. may be used.
[0660]Although the current impressed to the technical problem of this invention at EL element 15 is instant-like, there is a problem that it is N times larger as compared with the former. If current is large, the life of an EL element may be reduced. In order to solve this technical problem, it is effective to impress the reverse bias voltage Vm to EL element 15.
[0661]Hereafter, the method of impressing the reverse bias voltage Vm is explained. In order to impress the reverse bias voltage Vm, in the composition of drawing 6, it is necessary to control individually the gate terminal of TFT11b for a drive, and TFT11c for taking in. That is, it is necessary to make TFT11b for a

drive, and TFT11c for taking in turn on and off individually. This control method is explained using Drawing 131.

[0662]First, and TFT11d for switching is made one as shown in Drawing 131 (a) (drawing 6 is also united and it is a thing of reference). [TFT11c for taking in] And it is impressed by a terminal of the reverse bias voltage Vm and EL element 15. The reverse bias voltage Vm is the voltage lower than the cathode voltage Vs within more than 5V15V.

[0663]When EL element 15 lights up, the high voltage within more than 5V15V is impressed to a terminal to the cathode voltage Vs. That is, an absolute value impresses polar reverse voltage equally ideally to the voltage impressed when EL element 15 is on in the reverse bias voltage Vm. Since it is difficult, that an absolute value impresses polar reverse voltage equally actually impresses one 2 to 3 times the voltage of this with reverse polarity. EL element 15 stops as mentioned above, almost deteriorating by impressing the reverse bias voltage Vm.

[0664]Next, TFT11d for switching is turned off and TFT11b for a drive is made one as shown in Drawing 131 (b). And the black display voltage Vb is written in the capacitor 19. Drawing 110 explains this operation. Next, as shown in Drawing 131 (c), the on-off state of TFT11 is in the same state as Drawing 131 (b), and writes the image display voltage (current) from the current source 402 in the capacitor 19. Drawing 110 also explains this operation. Finally, as shown in Drawing 131 (d), turn off TFT11b for a drive, and TFT11c for taking in, and TFT11d for switching is made one, current is sent through EL element 15 and it is switched on.

[0665]The above operation is shown in Drawing 132. The reverse bias voltage Vm is impressed to the source signal line 18 in t 1 hour of 1H period, and the black display voltage Vb is impressed to the t2 next period, and the image data Vw (Iw) is impressed during t tertiary stage. Since Drawing 131 explains other operations and drawing 37, such as a drive method, drawing 38, etc. explain them, they omit explanation.

[0666]In the composition of Drawing 123, Drawing 124, Drawing 131, and Drawing 133, when incorporating the current of the source signal line 18 into the pixel 16, a reverse current flows into EL element 15. Therefore, when EL elements 15 are organic electroluminescence devices, it becomes possible like [at the time of impressing reverse voltage] to make late electrochemical degradation by the oxidation-reduction reaction of an organic molecule, etc.

[0667]The energy diagram of the three-layer type organic light emitting element which consists of the anode / electron hole transporting bed / luminous layer / an electron transport layer / the negative pole is shown in Drawing 134. The action of the positive/negative career at the time of luminescence is expressed with Drawing 134 (a). An electron hole is also poured into an electron hole transporting bed from the anode (anode) at the same time an electron is injected into an electron transport layer from the negative pole (cathode). The poured-in electron and an electron hole are moved to a counter electrode by an impressed electric field. In that case, into an organic layer, a trap is carried out or a career is accumulated by the difference of the energy level in a luminous layer interface.

[0668]Since the radical negative ion molecule or radical positive ion molecule by which it was oxidized or returned and the molecule was generated is unstable when space charge is accumulated into an organic layer, causing the fall of luminosity and the rise of the driver voltage at the time of a constant current drive due to deterioration of membraneous quality is known. In order to prevent this, device structure is changed as an example and reverse voltage is impressed.

[0669]Since a reverse current is impressed in Drawing 134 (b), the electron and electron hole which were poured in are drawn out to the negative pole and the anode, respectively. Thereby, the space charge formation in an organic layer is canceled, and it becomes possible to lengthen a life by suppressing electrochemical degradation of a molecule.

[0670]Although explanation about a three-layer type element was given in Drawing 134, also in the multilayer type element more than a four-layer type, and the element below a two-layer type, it is same that electrochemical degradation of an organic layer takes place by the electron and electron hole which were poured in from the electrode. Therefore, it becomes possible not to be based on the number of layers but to lengthen a life by this example. Since electrochemical degradation of a molecule is similarly produced in the element which mixed two or more materials with one layer, it is effective.

[0671]Even if the feature in this invention gives the function to send the bias current for preventing the waveform provincial accent by the stray capacitance which gives the function which prevents degradation of an organic molecule in this way, and is parasitic on a source signal line, it is being able to display without making a transistor count required for a pixel increase. That is, that it is not necessary to increase the number of the transistors for sending a reverse current has led to the advantage that it is not necessary to lower the numerical aperture of each pixel of a display.

[0672]The impression effect of the reverse bias voltage Vm is explained in Drawing 135. Drawing 135 shows the light emitting luminance of EL element 15 when it drives with predetermined current, and the terminal voltage of the EL element. In Drawing 135, the dotted line b shows the terminal voltage of EL element 15 when the reverse bias voltage Vm is impressed to EL element 15. The dashed dotted line c shows the terminal voltage of EL element 15 when the reverse bias voltage Vm is not impressed to EL element 15. The solid line a shows the light-emitting-luminance ratio (ratio when initial luminance is set to 1) of EL element 15 when (solid line a) the reverse bias voltage Vm is impressed to EL element 15.
[0673]In Drawing 135, an EL element is R luminescence and, specifically, is a case where a current drive is carried out in current density 100A / square meter. The sample B is impressing the current of current density 100A / square meter continuously during the time t. Although terminal voltage became high in lighting-times 1500 hours, brightness lowering was carried out rapidly, and after 2500-hour progress, only about 15% of luminosity was obtained to initial luminance.
[0674]The sample A carried out a 30-Hz pulse drive, sent the current of current density 200A / square meter at the half time t2, and impressed reverse-bias-voltage-14V to the time t1 of the half of the second half (it is got blocked and the average light emitting luminance per unit time is the same with the samples A and B). The lighting times from which the sample A will not almost have change of the terminal voltage of EL element 15 as the dotted line b shows, and luminosity will be 50% were 4000 hours.
[0675]Thus, even if it impresses the reverse bias voltage Vm, there is no increase in the terminal voltage of EL element 15, and there are few reduction rates of light emitting luminance. Therefore, the long lasting drive of EL element 15 is realizable.
[0676]Drawing 136 shows change of the reverse bias voltage Vm and the terminal voltage of EL element 15. This terminal voltage is a time of impressing amperage rating to EL element 15. Although Drawing 136 showed the case where the current sent through EL element 15 was current density 100A / square meter, the tendency of Drawing 136 did not almost have a difference with the case of current density 50-100A / square meter. Therefore, it is presumed that it is applicable with the current density of the wide range.
[0677]A vertical axis is a ratio with the terminal voltage 2500 hours after receiving the terminal voltage of early EL element 15. For example, in lapsed time 0 hour, terminal voltage when the current of current density 100A / square meter impresses will be set to 8V, and in lapsed time 2500 hours, if terminal voltage when the current of current density 100A / square meter impresses is set to 10V, a terminal voltage ratio will be 10/8=1.25.
[0678]A horizontal axis is a ratio of the reverse bias voltage Vm to the rated terminal voltage V0 to the product of the time t1 which impressed reverse bias voltage to one cycle. For example, it is t1=0.5 if the time which impressed the reverse bias voltage Vm at 60 Hz is 1/2. If terminal voltage (rated terminal voltage) when the current of current density 100A / square meter impresses is set to 8V in lapsed time 0 hour and reverse bias voltage Vm is set to 8V, | It is set to reverse-bias-voltage xt1|/(rated terminal voltage xt2) =|-8Vx0.5|/(8Vx0.5) =1.0.
[0679]According to Drawing 136, | reverse-bias-voltage xt1|/(rated terminal voltage xt2) of change of a terminal voltage ratio is lost by more than 1.0 (it does not change from early rated terminal voltage), and the effect by impression of the reverse bias voltage Vm is often demonstrated. However, since | reverse-bias-voltage xt1|/(rated terminal voltage xt2) tends to increase a terminal voltage ratio by more than 1.75, It is good to determine that the size and the applying time ratio t1 (or ratio of t2, or t1 and t2) of the reverse bias voltage Vm will become 1.75 or less preferably 1.0 or more.
[0680]However, to perform a bias drive, it is necessary to impress the reverse bias voltage Vm and amperage rating by turns. To impress the reverse bias voltage Vm if it is going to make equal average luminance per unit time with the samples A and B as shown in Drawing 135, it is necessary to send current high in instant as compared with the case where it does not impress. Therefore, terminal voltage of EL element 15 in the case (the sample A of Drawing 135) of impressing the reverse bias voltage Vm must also be made high.
[0681]However, let rated terminal voltage V0 be the terminal voltage (terminal voltage which is got blocked and turns on EL element 15) which fills average luminance in Drawing 136 also with the drive method which impresses reverse bias voltage (according to the example of this specification, it is terminal voltage when the current of current density 200A / square meter is impressed.). However, since it is 1/2 duty, the average luminance of one cycle turns into luminosity in current density 200A / square meter.
[0682]The above matter assumes the case of a white raster display for EL element 15 (when maximum current is being impressed to the EL element of the whole screen), but when performing graphic display of an EL display, is natural drawing and performs a gradation display. Therefore, it is white peak current (current which flows by the maximum white display.) of EL element 15 continuously. In the example of this

specification, the current of average current density 100A / square meter is not necessarily flowing.
[0683]The current (flowing current) generally impressed to each EL element 15 when performing graphic display is white peak current (current which flows at the time of rated terminal voltage.). Since it is about 0.2 time the current of current density 100A / square meter according to the example of this specification, to perform graphic display, in the example of Drawing 136, it is necessary to increase the value of a horizontal axis 0.2 time. Therefore, | reverse-bias-voltage xt1|/(rated terminal voltage xt2) is good to determine that the size and the applying time ratios t1 of the reverse bias voltage Vm (or ratio of t2, or t1 and t2, etc.) will become more than 0.2. | reverse-bias-voltage xt1|/(rated terminal voltage xt2) is good preferably to determine that a size, the applying time ratio t1, etc. of the reverse bias voltage Vm will become less than 1.75x0.2=0.35.
[0684]That is, since it is necessary to set the value of 1.0 in the horizontal axis (| reverse-bias-voltage xt1|/(rated terminal voltage xt2)) of Drawing 136 to 0.2, an image is displayed on a display panel (this condition of use will be usual.). When always not displaying a white raster, it is made to impress the reverse bias voltage Vm to the predetermined time t1 so that | reverse-bias-voltage xt1|/(rated terminal voltage xt2) may become larger than 0.2. Even if the value of | reverse-bias-voltage xt1|/(rated terminal voltage xt2) becomes large, as illustrated in Drawing 136, there is no increase in a terminal voltage ratio so much. Therefore, what is necessary is to also take carrying out a white raster display into consideration, and just to make it, as for upper limit, the value of | reverse-bias-voltage xt1|/(rated terminal voltage xt2) fill 1.75 or less.
[0685](Embodiment 9) The reverse bias method of this invention is explained hereafter, referring to drawings. Although this invention is based on impressing the reverse bias voltage Vm (current) to the period when current is not flowing into EL element 15, it is not limited to this. For example, the reverse bias voltage Vm may be compulsorily impressed in the state where current is flowing into EL element 15. In this case, as a result, current will not flow into EL element 15, but it will be in the astigmatism light state (black display state). Although this invention is explained focusing on impressing the reverse bias voltage Vm mainly by the pixel configuration of current programming, it is not limited to this. For example, TFT11e is made to turn off in drawing 76, and if it has composition which impresses the reverse bias voltage Vm to the anode of EL element 15 like Drawing 137, the impression of the reverse bias voltage Vm explained below is easily realizable also by the pixel configuration of a voltage program method. Therefore, the effect explained with Drawing 136 etc. can be demonstrated.
[0686]Drawing 137 is an explanatory view of the drive method of the reverse-bias-voltage impression method of this invention. Drawing 137 arranges or forms TFT11g for switching which impresses the reverse bias voltage Vm to the pixel configuration of drawing 6 (a). The gate terminal of TFT11g for switching is connected to the gate signal line 17d for control. The reverse bias voltage Vm is impressed to the anode of EL element 15 by making TFT11g for switching one.
[0687]First, one [TFT11b for a drive, and TFT11c for taking in] if ON state voltage Vgl is impressed to the gate signal line 17a as shown in Drawing 138 (a1). Then, as shown in Drawing 138 (a2), the program current Iw flows into TFT11c for taking in, etc. from the source driver 14, and current programming is carried out to the capacitor 19. Although not limited N times, in order to explain easily here, N times as much current shall be programmed and only the period of 1 F/N shall send the current Id through EL element 15.
[0688]Next, OFF state voltage Vgh is impressed to the gate signal line 17b, and TFT11b for a drive and TFT11c for taking in turn off so that it may illustrate to Drawing 138 (b1). being simultaneous (not limited simultaneously) -- one [TFT11d for switching] if ON state voltage Vgl is impressed to the gate signal line 17b. Then, as shown in Drawing 138 (c2), the current Id to which current programming of the power supply Vdd was carried out via TFT11a for conversion flows into EL element 15, and EL element 15 emits light so that it may illustrate to Drawing 138 (c1). This light emitting luminance will emit light by one about N times the luminosity of this, if the conversion efficiency of a program is 100%.
[0689]A light emission period is 1 F/N. TFT11d for switching is an OFF state during the remaining periods of 1F (1-1/N), and EL element 15 serves as astigmatism light (black display). At the time of astigmatism light, since current does not flow into EL element 15 at all, a perfect black display is rcalizable. At the time of luminescence, since white peak current is large, light emitting luminance is also high. Therefore, in the drive method of this invention, a very high contrast display is realizable.
[0690]If it is going to realize a black display when 1 time as much current is sent through all the periods of 1F at EL element 15 (the conventional drive method), it is necessary to program black display current to the capacitor 19. However, in a current drive method, since the current value at the time of a black display is small, the technical problem that it is greatly influenced by parasitic capacitance and sufficient resolution

does not come out and that it is generated by the black float occurs. Moreover, it runs from the gate signal line 17, and is influenced by voltage. By these technical problems, as for a black indicator, EL element 15 will be in a fine lighted condition, and contrast gets very bad.

[0691]In the drive method of this invention, since current does not flow through the period of 1F (1-1/N) into EL element 15 thoroughly, a perfect black display is realizable. That is, it is not generated by the black float. Therefore, even if it does not perform precharge for the black display explained with Drawing 131 etc., a high contrast display is realizable.

[0692]It cannot be overemphasized that methods, such as Drawing 131, may be added and enforced to the method explained with Drawing 137 etc., of course. Realization of a high contrast display demonstrates an effect similarly in the pixel configuration of voltage programs, such as drawing 76. That is, by carrying out 1 F/N pulse drive, current does not flow into EL element 15 at all, but the period of 1F (1-1/N) can realize a high contrast display.

[0693]ON state voltage is impressed to the gate signal line 17d, and TFT11g for switching is made one so that it may illustrate to Drawing 138 (d1). TFT11d for switching is made into an OFF state at this time. By making TFT11g for switching one, it is an anode (in addition depending on a pixel configuration, the reverse bias voltage Vm may be impressed to the cathode of EL element 15.) of EL element 15. The reverse bias voltage Vm is the reverse bias voltage Vm (it can express, even if the reverse bias current Im flows.) for there being a case of the voltage of straight polarity. It is because it can be considered in circuit that EL element 15 is a capacitor, so current flows in exchange by impression of the reverse bias voltage Vm. moreover -- since the accumulated electric charge is discharged -- it is -- it is impressed. The time t1 to impress is constituted so that the state of Drawing 136 may be fulfilled (Drawing 138 (d2)).

[0694]As for the period which impresses this reverse bias voltage Vm, it is preferred to consider it as the period when the current Id is not flowing into EL element 15. Although it is not an impossible reason, it is because it will be in the reverse bias voltage Vm and a short condition if the current Id is flowing.

[0695]in addition -- the period which impresses the reverse bias voltage Vm in Drawing 138 (d1) is not what is limited to this although one of 1F places was used -- two or more division (for example, the reverse bias voltage Vm is impressed to EL element 15 in 2 times or more or 3 steps or more during 1F) -- it may carry out.

[0696]Since what is necessary is just to impress on-off voltage to the gate signal line 17d to arbitrary timing among the periods which are impressing OFF state voltage to the gate signal line 17b, this control can be performed easily. And what is necessary is just to make it total of such ON time be t 1 hour explained with Drawing 136.

[0697]The period 1F (1-1/N) which does not send current through EL element 15 may be divided in two or more periods. Generating of a flicker is controlled by dividing into plurality. What is necessary is just to impress the reverse bias voltage Vm to that period, when this period 1F (1-1/N) is divided into plurality. However, it is not necessary to impress the reverse bias voltage Vm to all the divided periods 1F (1-1/N).

[0698]It amends below based on the contents explained with Drawing 136 about the drive method which does not impress reverse bias voltage and with which current is not flowing into EL element 15 as shown in Drawing 135 (or supplement). The time t1 explained with Drawing 136 is the time which impressed the reverse bias voltage Vm. The time t2 is the time which impressed current to EL element 15.

[0699]The reverse bias voltage Vm does not need to be a fixed value (Vm=-8V) in direct current. That is, the reverse bias voltage Vm is good also as a signal of a teeth-of-a-saw waveform, and good also as a wave-like pulse signal. The signal wave form of a sine wave may be used. Reverse bias voltage in this case is used with the thing which integrated with the waveform, or an effective value. What is necessary is to use as a square wave form what integrated with the reverse bias voltage Vm, and an effective value, and just to set time to suppose that this square wave form was impressed to t1, although the applying time t1 is also indefinite.

[0700]For example, the waveform of reverse bias voltage presupposes that a maximum amplitude value is 16V and applying time is t1=100microsec by the voltage waveform (triangle wave) illustrated to Drawing 139 (a). In this case, 8V and applying time have a maximum amplitude value equivalent to t1= 100micro sec of voltage waveform so that it may illustrate to Drawing 139 (b). A maximum amplitude value may process by considering that 16V and applying time are equivalent to t1= 50micro sec of voltage waveform so that it may illustrate to Drawing 139 (c). The above matter is the same also about the voltage for Masakata impressed by EL element 15.

[0701]The same matter corresponds also about the current Id sent through EL element 15. That is, what is necessary is to also use as the current wave form of a sine wave form instead of a direct current, etc. the current (voltage) sent through EL element 15, to change it into the effective value of a direct current also

in this case, and just to convert it into the applied period t2 of that square wave.
[0702]The period which impresses the reverse bias voltage Vm is good also as all the periods other than the period (usually 1H period : program period) which impresses ON state voltage to the gate signal line 17a so that it may illustrate to Drawing 140 (a).
[0703]Since what is necessary is just to impress the reverse bias voltage Vm to the period which is not impressing the current Id to EL element 15, So that it may illustrate to Drawing 140 (b), So that the reverse bias voltage Vm may be impressed to the period containing the period (program period) which impresses ON state voltage to the gate signal line 17a. It may constitute (Drawing 140 (b) is impressing the reverse bias voltage Vm in addition to the period (period which is impressing ON state voltage to the gate signal line 17b) which is impressing the current Id to EL element 15).
[0704]The matter about the applying time of the reverse bias voltage Vm explained with Drawing 138, Drawing 140, etc., an impression method, applying timing, etc. is applied to other examples.
[0705]As mentioned above, in this invention, it has the astigmatism light period (non display regions) 312 in 1F period, and by providing this astigmatism light period, animation display performance improves and the reverse bias voltage Vm can be impressed to EL element 15 during the astigmatism light. Therefore, since EL element 15 does not deteriorate and there is also no rise of terminal voltage, the power supply voltage Vdd can be set up low.
[0706]Drawing 140 was constituted so that the reverse bias voltage Vm might be impressed just before EL element 15, but as other composition, the composition which impresses the reverse bias voltage Vm (current-Im) to EL element 15 via TFT11d for switching is also illustrated so that it may illustrate to Drawing 141.
[0707]By impressing ON state voltage to the gate signal line 17d, and the reverse bias voltage Vm is impressed. [TFT11g for switching] By making TFT11d for switching one simultaneously, the reverse bias voltage Vm can be impressed to EL element 15. If it is the composition of Drawing 141, since it is controllable by TFT11g for switching, and 11-d both, control will become easy and pliability of impression of the reverse bias voltage Vm will improve.
[0708]When the applicable pixel is chosen, ON state voltage is impressed to the gate signal line 17. OFF state voltage is impressed to the period of non selection. Therefore, since OFF state voltage is impressed to almost all periods among the periods of 1F, the voltage impressed to a gate signal line can use OFF state voltage as reverse bias voltage.
[0709]OFF state voltage is usually potential lower than cathode voltage in order to make TFT turn off thoroughly (of course, when TFT is P channel, it is reverse). Especially when TFT is an amorphous silicon, usually OFF state voltage is set up quite low.
[0710]In the composition of Drawing 142, TFT11b for a drive connected to the gate signal line 17a and TFT11c for taking in are used as the N channel TFT. Therefore, and it will be in an OFF state with OFF state voltage Vgl. [ON state voltage Vgh] [TFT11b for a drive, and TFT11c for taking in] OFF state voltage Vgl is impressed to almost all the periods of 1F, and the gate signal line 17b. Let this OFF state voltage Vgl be the reverse bias voltage Vm (Vgl=Vm).
[0711]TFT11g for switching as well as a previous example is controlled by voltage impressed to the gate signal line 17d. Although refused, since the voltage impressed to the gate signal line 17d controls turning on and off of TFT11g for switching, the voltage to impress is not specified as Vgh and Vgl and can use other arbitrary voltage.
[0712]One of TFT11g for switching will impress OFF state voltage Vgl currently impressed to the gate signal line 17a to EL element 15. Therefore, the reverse bias voltage Vm can be impressed to EL element 15. In the composition of Drawing 142, since the signal wire which supplies the reverse bias voltage Vm as shown in Drawing 141 is unnecessary, a pixel numerical aperture can be improved. In Drawing 142, it may constitute so that the voltage impressed to the gate signal line 17b may be impressed to EL element 15 (TFT11d for switching needs to take composition, such as using N channel, into consideration).
[0713]Although Drawing 142 showed the composition which makes voltage of the gate signal line 17 reverse bias voltage, Drawing 143 shows the composition which makes voltage impressed to the source signal line 18 the reverse bias voltage of EL element 15. To the timing [one / timing / TFT11g for switching], if the reverse bias voltage Vm is impressed to the source signal line 18, the reverse bias voltage Vm can be impressed also to EL element 15 through the source signal line 18. Since Drawing 131 explains, timing is omitted.
[0714]Since the voltage charged by EL element 15 is discharged so that it may illustrate to Drawing 144, when long [time to impress the reverse bias voltage Vm] as compared with the period which is impressing current to EL element 15, there is an effect also in making between the anode terminal of EL element 15,

and a cathode terminal short-circuit. By making it short-circuit in this way, the electron which the electron hole accumulated in the electron hole transporting bed of EL element 15 was drawn out, and was accumulated in the electron transport layer is also drawn out, and degradation of an EL element can be controlled now. It cannot be overemphasized that the matter about the applying time of the reverse bias voltage Vm explained with Drawing 138, Drawing 140, etc., an impression method, applying timing, etc. is applied to the example of Drawing 144, etc.

[0715]Although each TFT was constituted from Drawing 144 by P channel, the composition of Drawing 144 is changed to N channel in Drawing 145. In Drawing 145, if one [TFT11g for switching], between the anode terminal of EL element 15 and a cathode terminal will short-circuit, and Vdd voltage will be impressed to both this terminal. The electron which the electron hole accumulated in the electron hole transporting bed of EL element 15 in this period was drawn out, and was accumulated in the electron transport layer is also drawn out, and degradation of an EL element can be controlled now. It cannot be overemphasized that the matter about the applying time of the reverse bias voltage Vm explained with Drawing 138, Drawing 140, etc., an impression method, applying timing, etc. is applied to the example of Drawing 145, etc. like Drawing 144.

[0716]The reverse bias voltage Vm can be impressed to EL element 15 also by changing the control directions through which current flows. Drawing 146 is the lineblock diagram. 402 in Drawing 146 is a constant current source.

[0717]In Drawing 146, when one [TFT11g for switching], the current of the constant current source 402 and a uniform direction flows into TFT11g for switching, and forward voltage is impressed to EL element 15. On the other hand, since a loop is constituted from EL element 15 and the constant current source 402 when TFT11g for switching is OFF, the direction of current which flows into EL element 15 becomes reverse. That is, the reverse bias voltage Vm can be easily impressed to EL element 15 by control of TFT11g for switching by arranging or forming the constant current source 402. The timing of the gate signal line 17 at this time is shown in Drawing 147. ON state voltage is impressed to the gate signal line 17d in periods other than the period when the gate signal line 17a is chosen. In this way, the electron which the electron hole accumulated in the electron hole transporting bed of EL element 15 was drawn out, and was accumulated in the electron transport layer is also drawn out, and oxidation of a hole transporting material and degradation by reduction of an electron transport material can be controlled now.

[0718]When Drawing 148 uses TFT11g for switching as N channel, it makes TFT11g for switching an OFF state when one [TFT11d for switching], and TFT11d for switching turns off, it is the composition which made TFT11g for switching the ON state. When one [TFT11d for switching], EL element 15 lights up, and when one [TFT11g for switching], the reverse bias voltage Vm is impressed to EL element 15.

[0719]As for the reverse bias voltage Vm, it is effective to use voltage lower than the cathode voltage Vk. However, a generation circuit is required if it is going to generate the reverse bias voltage Vm separately. With Drawing 149, the premature start capacitor is formed to this technical problem. The premature start capacitor 1001 is arranged for every pixel (formation), and also it may arrange one circuit on a panel (formation).

[0720]The premature start capacitor 1001 is operated by controlling the gate signal lines 17e and 17f. And the gate signal line 17e and the gate signal line 17f are operated by an opposite phase.

[0721]First, ON state voltage is impressed to the gate signal line 17e, TFT11i and 11j are made one and Vdd voltage is impressed to the capacitor 19b. OFF state voltage is impressed to the gate signal line 17f, and the capacitor 19b is made to turn off TFT11h and 11k after charge at this time.

[0722]Next, OFF state voltage is impressed to the gate signal line 17e, TFT11i and 11j are made to turn off, ON state voltage is impressed to the gate signal line 17f, and TFT11h and 11k are made one. Then, the Vdd voltage charged by the capacitor 19b serves as an opposite phase, and impresses -Vdd voltage to EL element 15.

[0723]Vm voltage (Vm=-Vdd) of an opposite phase can be generated by constituting as mentioned above. Therefore, supply wiring of Vm voltage becomes unnecessary.

[0724]It cannot be overemphasized that the pixel configuration of a current mirror can also be constituted so that the reverse bias voltage Vm can be impressed so that it may not be limited to this although the above example illustrates and explains the pixel configuration of the current programming method explained mainly by drawing 6, and it may be illustrated to Drawing 150. Since the operation can apply correspondingly the composition explained with Drawing 137 as it is, it is omitted. As illustrated to Drawing 151, even if it is a pixel configuration of a voltage program, it cannot be overemphasized that reverse bias voltage can be impressed. Drawing 76 is also the same. Therefore, the composition or the method of a voltage program that a pixel configuration also impresses reverse bias voltage to EL element 15 at the time

of astigmatism light is applicable.
[0725]In the above example, this invention explained noting that it was the composition or the method of impressing the reverse bias voltage Vm to EL element 15 at the time of astigmatism light. This displays the display screen 21 and is not limited to impressing the reverse bias voltage Vm to EL element 15 at the time of the astigmatism light of EL element 15. In an active-matrix type EL display panel, the composition which impresses the reverse bias voltage Vm continuously at the time of astigmatism light is also a category of this invention.
[0726]For example, during a prescribed period, after use of an EL display panel is completed, it may constitute so that the reverse bias voltage Vm may be impressed to EL element 15 of all the display screens 21. After ending use of an EL display panel, it may constitute during a prescribed period so that EL element 15 of all the display screens 21 may be scanned sequentially and the reverse bias voltage Vm may be impressed. When using an EL display panel (at for example, the time of the power supply ON), it may constitute during predetermined time so that EL element 15 of all the display screens 21 may be scanned sequentially and the reverse bias voltage Vm may be impressed. While not using the EL display panel, it may constitute so that the reverse bias voltage Vm may be impressed to every predetermined time interval (like [for 10 seconds] for every [for example,] hour). On the contrary, while using the EL display panel, it may constitute so that the reverse bias voltage Vm may be impressed to every predetermined time interval (like [for 10 seconds] for every [for example,] hour).
[0727]In Drawing 127, TFT11 which constitutes a pixel is five pieces. However, at drawing 6 (a), it comprises four pieces. Therefore, since there are few a TFT11 numbers with which the direction of the composition of drawing 6 (a) constitutes the pixel 16, a numerical aperture can be made high and there is an advantage that there are few generation ratios of a picture element defect.
[0728]Drawing 130 also shows the pixel configuration of a current programming method. Current programming can be performed by impressing ON state voltage to the gate signal line 17a. The current programmed by EL element 15 can be sent by impressing OFF state voltage to the gate signal line 17b, and impressing ON state voltage to the gate signal line 17b.
[0729]By impressing ON state voltage or OFF state voltage to the gate signal line 17c also in the composition of Drawing 130, the current sent through EL element 15 can be controlled, and the drive method or displaying condition illustrated to drawing 38 etc. can be realized.
[0730]Although TFT11e was added in Drawing 130, it cannot be overemphasized by deleting this TFT11e, operating the gate signal line 17b, and controlling the on-off state of TFT11d for switching that image display, such as drawing 38, etc. are realizable.
[0731]Drawing 152 also shows the pixel configuration of a current programming method. Current programming can be performed by impressing ON state voltage to the gate signal line 17a. The current programmed by EL element 15 can be sent by impressing OFF state voltage to the gate signal line 17b, and impressing ON state voltage to the gate signal line 17b.
[0732]Since turning on and off of TFT11d for switching is realizable by impressing ON state voltage or OFF state voltage to the gate signal line 17c also in the composition of Drawing 152, the current sent through EL element 15 is controllable. Therefore, the drive method or displaying condition illustrated to drawing 38 etc. is realizable.
[0733]Drawing 70 is an example of the pixel configuration of a voltage program. This invention is the method of obtaining predetermined light emitting luminance, by controlling the applying time of the current sent through the 1 field or the predetermined time of one frame (1F and, cutting 2F or more than it off the 1st division, of course are also considered) at EL element 15. That is, the current sent through an EL element is made higher than predetermined luminosity, and the amount of luminosity higher than predetermined is the method of obtaining predetermined luminosity, by shortening ON time.
[0734]Drawing 76 is also a pixel configuration by a voltage program. In drawing 76, 19a is the capacity for threshold detection (capacitor), and 19b is the capacity for input-signal-voltages maintenance (capacitor).
[0735]In Step 1 (section 1), since said TFT11a to all TFT11e is turned ON and said transistor for a drive is once made into the ON state, a gap of the current value by dispersion in a threshold occurs.
[0736]In Step 2 (section 2), since the current value of said TFT11a for a drive is set to 0 when said TFT11b and TFT11d turn OFF said TFT11c and TFT11e with ON, the threshold of said TFT11a for a drive is detected by said capacity 19a for threshold detection.
[0737]By turning OFF said TFT11b and TFT11d, and turning ON said TFT11c and TFT11e in Step 3 (section 3), The signal level which applied the threshold to said input signal voltages is impressed to the gate of said TFT11a for a drive, a current drive is carried out and EL element 15 is made to emit light at the same time it holds the input signal voltages of a data signal line in said capacity 19b for input-signal-

voltages maintenance. Since this TFT11a for a drive is operating in the saturation region, the current proportional to the square of the pressure value which lengthened the threshold from gate voltage flows, but since the threshold is already impressed to gate voltage with said capacity 19a for threshold detection, a threshold is canceled as a result. Therefore, even if the threshold of TFT11a for a drive varies, as shown in a simulation result, a fixed current value will always flow into EL element 15.

[0738]In Step 4 (section 4), when the pixel 16 enters during the non selection, even if TFT11b and TFT11d turn OFF TFT11c with ON, OFF and TFT11e, Since the input signal voltages held at said capacity 19b for input-signal-voltages maintenance and the threshold voltage held with said capacity 19a for threshold detection are impressed to the gate of TFT11a for a drive, current flows into EL element 15 and emitting light is continued.

[0739]As mentioned above, in order to detect the threshold of said transistor for a drive more correctly, it is required to set to less than more than 2microsec10microsec as a period of the 1st step, and to set to less than more than 2microsec10microsec as a period of the 2nd step. This is for writing in or fully securing operating time. However, if too long, original voltage program time will become short and stability will be lost.

[0740]Therefore, there is an effect in carrying out the drive method or display of this invention also by the voltage program method of drawing 70. TFT11d for switching can be made to turn on and off by controlling the gate signal line 17b in drawing 70. Therefore, the intermission of the current which flows into EL element 15 can be carried out. Also in drawing 76, on-off control of the TFT11e can be carried out by control of the gate signal line 17c. Therefore, displaying conditions, such as drawing 38 and drawing 42, are realizable.

[0741]It is clear that the drive method (not limited in addition to N times or 1/N) that 1/N carries out period lighting is realizable by increasing the current which flows into EL element 15 N times, and controlling the on-off state of TFT11e. That is, this invention is not limited only to the pixel configuration of the current programming of drawing 6, and the pixel configuration of voltage programs, such as drawing 76, can also realize the drive method of this invention. Therefore, the matter indicated on these specifications is applicable to a pixel configuration or a device indicated or illustrated on these specifications.

[0742]Similarly, drawing 74 and drawing 75 are also the pixel configurations of a voltage program. TFT11e can be made to turn on and off by controlling the gate signal line 17b in drawing 74 and drawing 75. Therefore, the intermission of the current which flows into EL element 15 can be carried out. Therefore, displaying conditions, such as drawing 38 and drawing 42, are realizable. Therefore, an animation effect is easily realizable. Variegated image display is realizable. Since other matters or operation is similar like drawing 76, it omits explanation. It cannot be overemphasized that the above matter is applicable also about the reverse-bias-voltage Vm impression method explained with Drawing 131, Drawing 137, etc.

[0743]For example, the reverse bias voltage Vm may change a pressure value for every R, G, and B pixel. In that case, the number of the gate signal line of TFT which controls the reverse bias voltage Vm increases. EL element 15 of each R, G, and B is because terminal voltage differs from force current, respectively. For example, it is the method of impressing -15V to the EL element of R pixel, and impressing -12V to the EL element of G and B pixel.

[0744]The applying time of the reverse bias voltage (current) impressed to EL element 15 of each R, G, and B may be changed. Respectively, it is because terminal voltage differs from force current for every RGB picture element. For example, it is the method that only one half of the time of 1F impresses the reverse bias voltage Vm to the EL element of R pixel, and only one third of the time of 1F impresses the reverse bias voltage Vm to the EL element of G and B pixel.

[0745]The applying time or impressed electromotive force of reverse bias voltage (current) may be changed for every portion of the display screen 21. For example, it is because the EL element of a center section has the large current value passed as compared with a periphery when the Gaussian distribution method which makes the center section of the display screen bright is adopted.

[0746]As a technical problem of a method that one N times the pulse voltage of this is impressed, the current which flows into EL element 15 becomes large, and the technical problem that EL element 15 deteriorates easily occurs. When it comes to N= 10 or more, the technical problem that it becomes high and power efficiency worsens also has the terminal voltage of EL element 15 which is needed when current flows. However, this technical problem is a technical problem generated when the current which flows into an EL element like [at the time of a white display] is large. The pixel configuration of drawing 6 is made into an example for the ways of coping to this technical problem, and it explains, referring to Drawing 153 (a).

[0747]While the current Idd to EL element 15 is flowing so that it may illustrate to Drawing 153 (a), the partial pressure of the Vdd voltage (power supply voltage) is carried out with the voltage Vsd between sauce drains of TFT11a for a drive, and the terminal voltage Vd of EL element 15. At this time, if Idd current is large, Vd voltage will also become high.
[0748]If Vdd voltage is high enough, the current Idd equal to the current Iw programmed by TFT11a for a drive will flow into EL element 15. Therefore, the current Iw and Idd is equal or becomes an almost linear relation (proportional relation) so that it may illustrate as the solid line of Drawing 154. I hear that poke to the capacitor 19 with the signal etc. which were impressed to the gate signal line 17 etc., an omission occurs, and it does not become Idd=Iw to become a linear relation, and there is.
[0749]In this invention, Vdd voltage is used on the low voltage which cannot maintain a relation of that Idd and Iw are linear (proportionality). That is, the relation of required Vsd+Vd>Vdd is used. It is preferred to consider it as Vd>Vdd.
[0750]For example, Iw current required for the maximum white display sets to 2microA by N= 10 as an example. In this state, since it will be set to Vd=14V in the EL element of G color if Idd current sets to 2microA, Vdd voltage at this time is made less than 14V. Or it will be referred to as Vd+Vsd=14V+7V=21 V<Vdd=21V at this time if Vsd=7V.
[0751]When it drives in this state, it stops being a relation with relation linear in the maximum white display between Iw and Idd in which the relation of the current Idd and Iw turns into a relation as shown by the dotted line of Drawing 154 (a nonlinear relation, the range of A of Drawing 154). However, in a black display or a gray display (field where display luminance is comparatively low), a linear relation (the range of B of Drawing 154) is maintained.
[0752]In the field of A, the current which flows into EL element 15 is restricted, and big current which degrades EL element 15 does not flow. Since Idd current will increase although there are few changing ratios if Iw current is made to increase in the field of A, a gradation display is realizable. However, in the field of A, since it becomes nonlinear, gamma conversion is required. For example, if image display is 64 gradation displays, table conversion of the inputted-image-data 64 gradation data will be carried out, it will be changed into 128 gradation or 256 gradation, and will be impressed to the source driver 14.
[0753]In the field of A, the partial pressure of the Vsd voltage of TFT11a for a drive and the Vd voltage of EL element 15 is carried out, and the terminal voltage Va of EL element 15 is determined. Under the present circumstances, since EL element 15 is formed by vacuum evaporation as a matter which should be observed (or spreading by ink jet art etc. formation), it is the point currently formed uniformly. Therefore, the EL terminal voltage Va serves as a uniform value in the field of the display screen 21. Therefore, the characteristic of TFT11a for a drive varies and it is amended with the terminal voltage Va of EL element 15. By making Vdd voltage low like this invention as a result, characteristic dispersion of TFT11a for a drive can be absorbed, and reduction of Vdd voltage can realize low power consumption. Also when large, high voltage is not impressed to EL element 15 for N.
[0754]EL element 15 can be formed not only with vacuum evaporation art and ink jet art but with the stamp art which applies the stamp which attached ink to paper and prints it.
[0755]First, the portion used as a stamp is formed. The pattern of the slot of the same form as the luminous region of an organic EL device is formed according to a semiconductor process on a Si substrate, and it is considered as a stamp by burying the material which dopes the inside of the slot to organic electroluminescence material. On the other hand, the organic electroluminescence material used as an electrode or a luminous layer is formed in the glass substrate of the direction which forms an organic EL device.
[0756]Next, the glass substrate which attached the material used as a stamp and an organic EL device is piled up exactly. It heat-treats over about 10 minutes at +100 ** - +200 **, maintaining this state. By carrying out like this, the doping materials embedded into the slot on the stamp evaporate, and it is spread in the luminous layer of an organic EL device. The rest applies the stamp embedding the doping materials according to a color to an organic EL device one by one, and distinguishes RGB by different color with. If this stamp art is used, EL element 15 of a 10 micrometers rectangular pattern and a pattern with a line width of 10 micrometers can form easily.
[0757]Current was impressed to 1/N of the period of 1F at EL element 15, the current to impress was made higher than predetermined luminosity, and the amount of luminosity higher than predetermined presupposed that it is the method of obtaining predetermined luminosity by shortening ON time. However, this invention is the method of making the luminance average within a fixed period a predetermined value. Therefore, it is not limited to 1F (1 field or one frame). For example, the displaying condition of drawing 42 (c1) may continue 2F, the displaying condition of drawing 42 (c2) may continue 3F, or the state of this

drawing 42 (c1) and drawing 42 (c2) may be repeated by turns. What is necessary is eventually, just to drive so that it may become desired average luminance by 5F.
[0758]Therefore, the technical idea of this invention is a method which generates the ON state and OFF state of EL element 15, repeats this ON state and OFF state by turns, and obtains predetermined display luminance by this repetition within a fixed period. Control is realized by controlling the on-off voltage of the gate signal line 17.
[0759]Although N times as much current as predetermined current is sent through the source signal line 18 and N times as much current as predetermined current is sent through EL element 15 during the 1/N period, this is unrealizable practically. It is because the signal pulse actually impressed to the gate signal line 17 runs to the capacitor 19 and cannot set a desired pressure value (current value) as the capacitor 19. Generally a pressure value (current value) lower than a desired pressure value (current value) is set to the capacitor 19. For example, even if it drives so that one 10 times the current value of this may be set up, only about 5-time current is set to the capacitor 19. The current which actually flows into EL element 15 also as N= 10 becomes the same as that of the case of N= 5. Therefore, this invention is the method of driving so that it may flow into EL element 15 through the current which sets up one N times the current value of this, and was proportional or corresponds N times (however, since the drive method explained with Drawing 154 is also enforced, limitation is difficult). Or it is a drive method which impresses larger current than a desired value to pulse form at EL element 15.
[0760]A current (voltage) program is performed for current (current which will become higher than request luminosity as it is if current is sent succeeding EL element 15) to TFT11a for a drive from a desired value (when illustrating drawing 6), By making into an intermission the current which flows into EL element 15, the light emitting luminance of a desired EL element is obtained.
[0761]If drawing 6 is illustrated (voltage program pixel configurations, such as drawing 76, drawing 74, drawing 75, Drawing 110, and Drawing 151, are also effective), TFT11a for a drive, 1st TFT11c for switching that sets up the signal (current, voltage) course which programs to this TFT for a drive (composition, arrangement, connection), In the pixel configuration possessing 2nd TFT11d for switching that sets up the course through which the current from TFT11a for a drive flows into EL element 15 (composition, arrangement, connection), Where [1st] (a course is set up) and 2nd TFT11d for switching is turned off (a course is cut), [said 1st TFT11c for switching] The 1st state of carrying out a current (voltage) program at said TFT for a drive, and the 2nd state, one [turn off said 1st TFT11c for switching (a course is cut), and / 2nd TFT11d for switching] (a course is set up), The 3rd state of turning off said 1st TFT11c for switching (a course is cut), and turning off 2nd TFT11d for switching (a course is cut) is carried out.
[0762]In an active-matrix type display panel, the current route which flows into EL element 15 from TFT11a for a drive During the prescribed period in an one-frame (1 field) period, Cutting or reduction (the current wave form which flows into EL element 15 is not limited to a rectangle or DC, and has a sine wave form etc.) Also when changing DC amplitude value, it is a certain thing which carries out and decreases the light emitting luminance of EL element 15 of at least one frame (1 field).
[0763]The operation which programs so that EL element 15 emits light by luminosity higher than a desired value to TFT11a for a drive, Said programmed signal (current) is passed to EL element 15, and it operates so that it may not flow into said EL element 15 at the prescribed period in an at least one-frame (1 field) period.
[0764]Or the current which flows into EL element 15 is restricted so that below the luminosity corresponding to the current programmed by TFT11a for a drive may become.
[0765]The operation and the average luminance (request luminosity) of one frame (1 field) which program so that EL element 15 emits light by luminosity higher than a desired value, It operates so that said below request luminosity (programmed luminosity (current)) may become at least in request luminosity, and said program current may not flow into said EL element 15. It is not limited to making the current which flows into EL element 15 turn on and off thoroughly.
[0766]For example, OFF or low-intensity luminescence can be carried out for (it is got blocked and current smaller than a predetermined value is flowing into EL element 15), and EL element 15 by making TFT11d for switching into a high resistance ON state in drawing 6. When EL element 15 is low-intensity luminescence, it is necessary to replace with dark (luminosity near gray or a black display) one instead of a perfect black display, and to understand in the non display regions 312 of the display screen 21. That is, what is necessary is just usually a low-intensity display from a display in the non display regions 312. The displaying condition which can recognize a picture to be a low-intensity display is also included.
[0767]As for the above example, it is effective to combine what (see Drawing 136, Drawing 138, etc.) reverse bias voltage is impressed to the astigmatism light time of EL element 15 for. It cannot be

overemphasized that it is effective also in voltage program pixel configurations, such as drawing 76.
[0768]In drawing 38 etc., the non display regions 312 do not completely need to be in an astigmatism light state. Even if weak luminescence or the image display carried out slightly occurs, it is satisfactory practically. That is, it should be interpreted as the field where display luminance is lower than the image display region 311. In the non display regions 312, also when only one color or two colors call it a non-display state among R, G, and B image display, it is contained.
[0769]In each pixel configuration (for example, drawing 70, Drawing 126, Drawing 152 (a)), even if it constitutes the gate terminal of TFT11d for switching so that on-off voltage can be impressed directly, the intermittent control action of the current sent through EL element 15 can be carried out. Even if it constitutes the gate terminal of TFT11b for a drive in TFT11a for conversion, and drawing 9 in TFT11e and drawing 8 in Drawing 127 so that on-off voltage can be impressed directly, the intermittent control action of the current sent through EL element 15 can be carried out. That is, by controlling the gate terminal of TFT which impresses current to EL element 15, I hear that displaying conditions, such as drawing 38, can be carried out, and it is.
[0770]As mentioned above, this invention indicates EL element 15 by intermittent by turning on and off the current impressed to EL element 15. In order to indicate by intermittent, it is necessary to carry out on-off control of the TFT11d for switching in the example of drawing 6. Therefore, the gate signal line for turning TFT11d for switching on and off is needed. That is, in order to indicate EL element 15 by intermittent, the 1st gate signal line for carrying out on-off control of the 1st switching element that forms the course for programming the current sent through EL element 15, and this 1st switching element is required for a capacitor. The 2nd gate signal line for turning on and off the 2nd switching element that forms the current route which flows into EL element 15, and this 2nd switching element is needed. That is, two gate signal lines per pixel are needed.
[0771]However, if two or more gate signal lines per pixel are needed, in the pixel configuration without three sides explained by drawing 13 etc., it will become a technical problem. Even if it forms the gate driver 12 with low-temperature-polysilicon art etc., it is because circuitry becomes the number of shift registers increases and complicated. If it is going to realize composition without three sides with amorphous silicon art especially, a technical problem will become large further. It is because the gate driver 12 (or source driver 14) cannot be directly formed on the display panel 82 with amorphous silicon art.
[0772]Therefore, in order to constitute a display panel from amorphous silicon art, it is necessary to arrange the source driver 14 and the gate driver 12 to one side of the display screen 21. And it is necessary to wave [gate signal line 17a and / all] to the right and left of a display screen 17b, to divide, and to wire. When there are few numbers of the gate signal line 17, it may still be able to correspond, but since a vertical pixel number is 220 dots also in QCIF, the gate signal line 17 will 220x2=440 become. In addition,-izing cannot be carried out [narrow picture frame], if there are many wiring numbers of the gate signal line 17 even when the gate driver 12 is built in with low-temperature-polysilicon art. Therefore, goods power will be lost.
[0773]This invention described from this solves the above-mentioned technical problem. If it indicates briefly, the gate signal line 17b which turns EL element 15 on and off will be carried out [two or more and]. This current that was carried out in common and that flows into EL element 15 for every block is turned on and off.
[0774]In the example of drawing 34 and drawing 84, it is not necessary to control one pixel row of turning on and off of EL element 15 at a time. It is because the non display regions 312 can be formed and the image display region 311 can also be formed, even if it turns on and off for every block. The method which carries out on-off control with a block as mentioned above is called a block drive. However, since there is also an example made a block by the pixel row which adjoined, from the concept of the usual block, it is a broad sense. However, it is necessary to change into an astigmatism light state the pixel row which is performing current programming in the pixel configuration of drawing 6. Therefore, it is necessary to make into the non display regions 312 the block including the pixel row selected for current programming. however, even if it is a case of drawing 6, when it sees in some pictures and permits whom, even if it is the pixel row which is performing current programming, it is not necessary to consider it as the non display regions 312 In the pixel configuration of the current mirror of drawing 8, even if it is the pixel row which is performing current programming, it is not necessary to consider it as the non display regions 312.
[0775]Although this invention explains by illustrating the pixel configuration of the current programming illustrated mainly to drawing 6, it is not limited to this, and even if it is other current programming composition (pixel configuration of a current mirror) explained by drawing 8 etc., it is applicable. The technical concept turned on and off with a block is applicable even if it is a pixel configuration of voltage

programs, such as drawing 75 and drawing 76. Since this invention is the method of making an intermission the current which flows into EL element 15, it is combinable also with the method which impresses the reverse bias voltage explained with Drawing 151 etc. As mentioned above, this invention can be carried out combining other examples.

[0776]Drawing 155 shows the example of a block drive. First, in order to explain easily, it is explained that form the gate driver 12 in the array substrate 49 directly, or it loads the gate driver 12 of a silicon chip into the array substrate 49. Since a drawing becomes complicated, the source driver 14 and the source signal line 18 are omitted.

[0777]The gate signal line 17a is connected with the gate driver 12 in Drawing 155. On the other hand, the gate signal line 17b of each pixel is connected with the light control line 1791. In Drawing 155, the four gate signal lines 17b are connected with the one light control line 1791. Blocking with the four gate signal lines 17b may not be limited to this, and it may be more than it. Generally, as for the display screen 21, it is preferred to divide into at least 5 or more and further 10 or more. Dividing or more into 20 is preferred. It is because the number of the light control line 1791 will increase and the layout of the light control line 1791 will become difficult, if a flicker can be seen easily when there is little number of partitions, and there is too much number of partitions.

[0778]Therefore, in the case of a QCIF display panel, since the number of a vertical scanning line is 220, it is necessary to block by or more 220 / 10= 11 preferably 5= 44 [220-/] or more at least. However, when two blocking is performed by odd lines and even lines, since there is comparatively little generating of a flicker also at a low frame rate, two blocking may be enough.

[0779]ON state voltage Vgl is impressed one by one with the light control lines 1791a, 1791b, 1791c, and 1791d, or OFF state voltage Vgh is impressed, and the current which flows into EL element 15 for every block is made to turn on and off in the example of Drawing 155.

[0780]In the example of Drawing 155, the gate signal line 17b and the light control line 1791 do not cross. Therefore, the short defect of the gate signal line 17b and the light control line 1791 is not generated. In order that the gate signal line 17b and the light control line 1791 may not carry out capacitive coupling, capacity addition when the gate signal line 17b side is seen from the light control line 1791 is very small. Therefore, it is easy to drive the light control line 1791.

[0781]Drawing 1 is illustrating the connected state of Drawing 155 still in detail. The gate signal line 17a is connected to the gate driver 12. By impressing ON state voltage Vgl to the gate signal line 17a, a pixel row is chosen, and, and they program the current (voltage) impressed to the source signal line 18 to the capacitor 19 of each pixel. [TFT11b which is each selected pixel, and 11c] On the other hand, the gate signal line 17b is connected with the gate terminal of TFT11d of each pixel. Therefore, when ON state voltage Vgl is impressed to the light control line 1791, the current route of TFT11a for a drive and EL element 15 is formed and OFF state voltage Vgh is impressed conversely, the anode terminal of EL element 15 is made open.

[0782]As for the control timing of the on-off voltage impressed to the light control line 1791, and the timing of the pixel row selection voltage Vgl which the gate driver 12 outputs to the gate signal line 17a, it is preferred to synchronize with 1 horizontal-scanning clock (1H). However, it is not limited to this. The signal impressed to the light control line 1791 makes the current to EL element 15 only turn on and off. The image data and synchronization which the source driver 14 outputs do not need to be taken. It is because the signal impressed to the light control line 1791 is what controls the current programmed by the capacitor 19 of each pixel 16. Therefore, the selection signal of a pixel row and the synchronization do not necessarily need to be taken. Even if it is a case where it synchronizes, a clock may not be limited to 1H signal, and 1/2H may be 1/4H.

[0783]Drawing 156 shows the case of the pixel configuration of the current mirror which the pixel configuration illustrated to drawing 8 etc. However, as the former example also explained, in order to control the current which flows into EL element 15, the gate signal line 17b for forming TFT11e and controlling TFT11e is added.

[0784]In Drawing 156, although the gate signal line which controls TFT11c for taking in and TFT11d for switching (turning on and off) was carried out in common (gate signal line 17a), it is not limited to this and is good also as the separate gate signal line 17. In this case, the 1st gate signal line 17 that controls TFT11c for taking in, and the 2nd gate signal line 17 that controls TFT11d for switching are connected to the gate driver 12.

[0785]The gate signal line 17a is connected to the gate driver 12 in Drawing 156. A pixel row is chosen by impressing ON state voltage to the gate signal line 17a. Although drawing 1 is also the same, the pixel row chosen is not limited to one pixel row. For example, two or more pixel line is chosen in drawing 83, drawing

86, and drawing 89. As mentioned above, this invention is not restrained by the number of pixel rows chosen.
[0786]In Drawing 156, if ON state voltage Vgl is impressed to the gate signal line 17a, and the current (voltage) impressed to the source signal line 18 will be programmed to the capacitor 19 of each pixel. [TFT11b for a drive of each selected pixel, and TFT11d for switching] That is, the source driver 14 outputs the current (voltage) written in the pixel 16 (absorption). On the other hand, the gate signal line 17b is connected with the gate terminal of TFT11e of each pixel. Therefore, when ON state voltage Vgl is impressed to the light control line 1791, the current route of TFT11b for a drive and EL element 15 is formed and OFF state voltage Vgh is impressed conversely, the anode terminal of EL element 15 is made open.
[0787]Drawing 157 shows the pixel configuration of a voltage program. However, as the former example also explained, in order to control the current which flows into EL element 15 (an intermittent control action can be carried out like), the gate signal line 17b for forming TFT11d for switching and controlling TFT11d for switching is added. This gate signal line 17b is connected to the light control line 1791 for two or more pixel line of every.
[0788]The gate signal line 17a is connected to the gate driver 12 in Drawing 157. By impressing ON state voltage to the gate signal line 17a, and a predetermined pixel row is chosen. [TFT11b for a drive]
[0789]In Drawing 157, if ON state voltage Vgl is impressed to the gate signal line 17a, and it will program the current (voltage) impressed to the source signal line 18 to the capacitor 19 of each pixel. [TFT11b for a drive of each selected pixel] That is, the source driver 14 outputs the current (voltage) written in the pixel 16 (absorption). On the other hand, the gate signal line 17b is connected with the gate terminal of TFT11d for switching of each pixel. Therefore, when ON state voltage Vgl is impressed to the light control line 1791, the current route of TFT11a for a drive and EL element 15 is formed and OFF state voltage Vgh is impressed conversely, the anode terminal of EL element 15 is made open.
[0790]Drawing 158 performs the intermittent control action of the current which flows into EL element 15 which is a pixel configuration of other voltage programs using TFT11d for switching. The gate signal line 17d for controlling TFT11d for switching is connected to the light control line 1791 for two or more pixel line of every.
[0791]In the pixel configuration of Drawing 158, in order to make the voltage which measured offset voltage and was written in the period of one frame hold to the capacitor 19, the two gate signal lines 17a and 17c are required. Therefore, these two gate signal lines 17a and 17c are connected to the gate driver 12. This composition is illustrated to Drawing 159. By impressing on-off voltage to the gate signal line 17a and the gate signal line 17c, the gate driver 12 carries out on-off control of TFT11c for taking in, and the TFT11b for a drive, and programs to a pixel the voltage outputted from the source driver 14. On the other hand, the gate signal line 17d is connected with the gate terminal of TFT11d for switching of each pixel. Therefore, when ON state voltage Vgl is impressed to the light control line 1791, the current route of TFT11a for a drive and EL element 15 is formed and OFF state voltage Vgh is impressed conversely, the anode terminal of EL element 15 is made open.
[0792]As mentioned above, this invention is applicable, even if a pixel configuration is a current programming method and it is a voltage program method. Although the above example illustrated and explained the active-matrix type display panel, it is not limited to this and can be applied also to a simple matrix type display panel. It is because a simple matrix type display panel is also realizable to carry out lighting or the astigmatism light of EL element 15 for every block.
[0793]Drawing 160 shows other examples. The following examples explain focusing on a difference with the example described previously. Therefore, an example or a pixel configuration after Drawing 160, etc. can also apply a gap to explain with drawing 1, Drawing 156 - Drawing 158, etc.
[0794]Drawing 160 shows the composition which carried out two pixel rows of gate signal lines 17b at a time in common, and was carried out in common by the light control line 1791 every 4 blocks. The gate signal line signal wire 17b of the 1st and the 2nd pixel row and the gate signal line 17b of the 9th and the 10th pixel row are carried out in common by the light control line 1791a. Therefore, if ON state voltage Vgl is impressed to the light control line 1791a, the at least 1st, the 2nd, the 9th, and the 10th pixel row will light up.
[0795]The gate signal line signal wire 17b of the 3rd and the 4th pixel row and the gate signal line 17b of the 11th and the 12th pixel row are carried out in common by the light control line 1791b. Therefore, if ON state voltage Vgl is impressed to the light control line 1791b, the at least 3rd, the 4th, the 11th, and the 12th pixel row will light up.
[0796]Similarly, the gate signal line signal wire 17b of the 5th and the 6th pixel row and the gate signal line

17b of the 13th and the 14th pixel row are carried out in common by the light control line 1791c. Therefore, if ON state voltage Vgl is impressed to the light control line 1791c, the at least 5th, the 6th, the 13th, and the 14th pixel row will light up. The gate signal line signal wire 17b of the 7th and the 8th pixel row and the gate signal line 17b of the 15th and the 16th pixel row are carried out in common by the light control line 1791d. Therefore, if ON state voltage Vgl is impressed to the light control line 1791d, the at least 7th, the 8th, the 15th, and the 16th pixel row will light up.

[0797]As shown in Drawing 160, if the gate signal line 17b is connected with the light control line 1791, a small lighting block will be displayed dispersedly. Therefore, generating of a flicker decreases also in a low rate.

[0798]Drawing 161 shows the composition which flew 4 pixels of gate signal lines 17b, and it came out of, was made common, and was connected to the light control line 1791. The gate signal line signal wire 17b of the 1st, the 5th, the 9th, and the 13th pixel row is carried out in common by the light control line 1791a. Therefore, if ON state voltage Vgl is impressed to the light control line 1791a, the at least 1st, the 5th, the 9th, and the 13th pixel row will light up.

[0799]The gate signal line signal wire 17b of the 2nd, the 6th, the 10th, and the 14th pixel row is carrying out in common by the light control line 1791b. Therefore, if ON state voltage Vgl is impressed to the light control line 1791b, the at least 2nd, the 6th, the 10th, and the 14th pixel row will light up.

[0800]The gate signal line signal wire 17b of the 3rd, the 7th, the 11th, and the 15th pixel row makes it the same in common by the light control line 1791c. Therefore, if ON state voltage Vgl is impressed to the light control line 1791c, the at least 3rd, the 7th, the 11th, and the 15th pixel row will light up. The gate signal line signal wire 17b of the 4th, the 8th, the 12th, and the 16th pixel row is carrying out in common by the light control line 1791d. Therefore, if ON state voltage Vgl is impressed to the light control line 1791d, the at least 4th, the 8th, the 12th, and the 16th pixel row will light up.

[0801]As shown in Drawing 161, if the gate signal line 17b is connected with the light control line 1791, the pixel row turned on rather than Drawing 160 will be distributed. Therefore, generating of a flicker decreases also in a low rate.

[0802]Drawing 162 shows the composition of having connected the gate signal line 17b of the odd number pixel row to the light control line 1791a, and having connected the gate signal line 17b of the even number pixel row to the light control line 1791b.

[0803]In Drawing 162, since the light control of EL element 15 can be carried out for every pixel row, generating of a flicker decreases also with a low rate. The light control line 1791 of 2 and a number decreases.

[0804]Drawing 163 shows the composition of having connected the gate signal line 17b to the light control line 1791a or the light control line 1791b every four pixel rows. In Drawing 163, it is easy to take the timing of the current (voltage) program to a pixel, and a synchronization.

[0805]With the voltage which impresses the above example to the light control line 1791, on-off control is performed for every pixel row, and an object of this invention is to carry out the intermittent control action of EL element 15. Therefore, it is not limited to the existence of the light control line 1791.

[0806]For example, the light control driver circuit 1891 is formed in one side of a display screen in Drawing 164 (arrangement). That is, the gate driver 12 was formed in one side of a display screen (arrangement), and the light control driver circuit 1891 is arranged to the confrontation of this neighborhood (formation). Using low temperature polysilicon or elevated-temperature polysilicon technology, the light control driver circuit 1891 may be directly formed in the array substrate 49, may be constituted from a silicon chip, and may use for and load COG technology etc. into the array substrate 49. However, as shown in Drawing 164, circuitry becomes very simple by being common in two or more gate signal lines 17b (blocking). Therefore, even if it forms in the array substrate 49 directly, it constitutes from a silicon chip, and even if it loads the array substrate 49, area is hardly occupied. Therefore, narrow picture frame-ization of a display panel is realizable. The light control driver circuit 1891 may be arranged the same neighborhood as the source driver 14, and three-side free composition may be realized.

[0807]Although the gate driver 12 was directly formed in the array substrate 49, or was constituted from a silicon chip using low temperature polysilicon or elevated-temperature polysilicon technology, and it was explained in the example to Drawing 164 that it used for and loaded COG technology etc. into the array substrate 49, This invention is not limited to this. For example, the gate signal line 17a may be wired from the neighborhood by which the source driver 14 has been arranged so that it may illustrate to Drawing 165. That is, both the light control line 1791 and the gate signal line 17a are formed in the end of the display screen 21. Since other composition is the same as that of Drawing 155 etc., explanation is omitted.

[0808]The source driver 14 and the gate driver 12 may be arranged in two neighborhoods of a display

screen, respectively (formation), and it may constitute so that it may connect with each gate driver 12 and source driver 14 in the center section of the display screen 21, so that it may illustrate to Drawing 166. By constituting in this way, leading about of the gate signal line 17a decreases (set to one half), and narrow picture frame-ization can be realized.

[0809]Drawing 167 is an explanatory view which has arranged the source driver 14, the gate driver 12, etc. on the panel. In Drawing 167, the source driver 14 was produced with the silicon chip, and it arranges to one side of the array substrate 49. The gate driver 12 is directly formed in the array substrate 49 using low temperature polysilicon, CGS art, or elevated-temperature polysilicon technology. The on-off voltage to the light control line 1791 is outputted from the source driver 14.

[0810]Drawing 168 shows the example which formed the light control driver circuit 1891 in the array substrate 49 directly using low temperature polysilicon, CGS art, or elevated-temperature polysilicon technology. Of course, the light control driver circuit 1891 may be produced with a silicon chip, and COG technology etc. may be used and loaded into the array substrate 49.

[0811]Drawing 169 shows the example which outputted the on-off signal to the light control line 1791 from control IC101 etc. Thus, even if the specification of the source driver 14 becomes simple and there is change to a drive method by constituting so that the on-off data of the light control line 1791 may be outputted from control IC101 of a microcomputer etc., etc., change of the source driver 14 becomes unnecessary.

[0812]Drawing 170 shows the composition using the gate driver 12a and the source driver 14a which drive the display screen 21a, and the gate driver 12b and the source driver 14b which drive the display screen 21b. Since other composition is the same as that of a former example, explanation is omitted.

[0813]Drawing 171 shows the example which outputted the on-off signal to the light control line 1791 from control IC101 etc., and formed the gate driver 12 and the source driver 14 in the array substrate 49 directly using low temperature polysilicon, CGS art, or elevated-temperature polysilicon technology. Of course, the source driver 14, the light control driver circuit 1891, etc. may be produced with a silicon chip, and COG technology etc. may be used and loaded into the array substrate 49.

[0814]Drawing 172 shows the composition that the on-off signal to the light control line 1791 outputted from control IC101 etc., and realized the image data to the control signal and the source signal line 18 to the gate signal line 17a with the source driver 14a. The source driver 14a may be directly formed in the array substrate 49 using low temperature polysilicon, CGS art, or elevated-temperature polysilicon technology. The source driver 14a etc. may be produced with a silicon chip, and COG technology etc. may be used and loaded into the array substrate 49.

[0815]In Drawing 141 - Drawing 150, etc., the method which the reverse bias voltage Vm impresses was explained. While the reverse bias voltage Vm was not impressing current to EL element 15 fundamentally, it was a method to impress. On the other hand, the block drive system explained by drawing 1 etc. forms the non display regions 312 and the image display region 311 for every block. Based on these, it can be impressed by EL element 15 of the non display regions 312 with the reverse bias voltage Vm by block drive. That is, reverse bias voltage (current) is impressed for every block. However, it is not limited to impressing the reverse bias voltage Vm to all blocks of the non display regions 312. For example, arbitrary blocks may be divided into plurality and the divided composition of impressing the reverse bias voltage Vm for every block may be used. Of course, non-display-regions 312 control is carried out for every block, and one pixel row of impression control of the reverse bias voltage Vm is good at a time in a line.

[0816]As mentioned above, by constituting so that the reverse bias voltage Vm may be impressed for every block, simple [of the pixel configuration etc. which were explained with Drawing 141 etc.] is carried out, and it becomes easy [control]. Logic is also easy in order to impress the reverse bias voltage Vm to the non display regions 312 especially.

[0817]Drawing 173 shows the example of this invention at the time of combining a block drive and a reverse-bias-voltage drive, and is the same as that of the pixel configuration of Drawing 141. This pixel configuration has combined the block drive explained by drawing 1. It cannot be overemphasized that it is applicable even if a block drive is the composition of a gap to explain with drawing 1, Drawing 156 - Drawing 172.

[0818]In Drawing 173, a corresponding block serves as the non display regions 312 by impressing OFF state voltage Vgh to the light control line 1791. It is simultaneous (not limited simultaneously.). which period may be sufficient as long as it is the period when OFF state voltage Vgh is impressed to the applicable light control line 1791 -- ON state voltage Vgl is impressed to the reverse bias control line 2111. Then, the reverse bias voltage Vm is impressed to EL element 15 of a corresponding block. That is, what is necessary is just to let the signal of the opposite phase of the light control line 1791 be the reverse bias

control line 2111 in logic.
[0819]Similarly, Drawing 174 shows the composition of having added the reverse bias drive system to the composition of Drawing 156. Drawing 175 shows the composition of having added the reverse bias drive system to the composition of Drawing 157, and Drawing 176 shows the composition of having added the reverse bias drive system to the composition of Drawing 158. Probably, operation does not have **** in explanation daringly, since it is easy.
[0820]Although indicated also in advance, impression of the reverse bias voltage Vm and the block drive do not need to take a synchronization thoroughly. It is not necessary to also coincide a scanning period thoroughly.
[0821]Hereafter, the block drive of this invention is explained succeedingly. Drawing 177 is an explanatory view of the block drive method of this invention. Also in subsequent explanatory views, in order to carry out easy [of the explanation], a pixel configuration is explained as a pixel configuration illustrated by drawing 6. However, it cannot be overemphasized that other pixel configurations, such as not the thing limited to this but drawing 8, drawing 75, and drawing 76, are good.
[0822]In the case of the pixel configuration of drawing 6, it is necessary to make into an OFF state TFT11d for switching of the pixel row which is performing current programming. that is, EL element 15 is not visible to a selected picture element line from the source signal line 18 -- as (EL element 15 is not connected to the source signal line 18) -- it drives. If absorbed, it will be to prevent the program current from the source signal line 18 from flowing into EL element 15. It is because it becomes impossible to program regular current to the capacitor 19 when program current flows in by EL element 15.
[0823]Therefore, when carrying out a block drive, it is necessary to make into the non display regions 312 the block containing a selected picture element line. That is, when the pixel row in a corresponding block is chosen, let this block be the non display regions 312 continuously. On the contrary, the image display region 311 or any of the non display regions 312 may be sufficient as other blocks. In order to control a flicker, it carries out by carrying out on-off control of the block of those other than this selected picture element line.
[0824]As for Drawing 177 (a), the one write-in pixel row 871a of the block 1981b is chosen. Therefore, the block 1981b is controlled by the astigmatism light state. If the block 1981 comprises six pixel rows, the selected block 1981 will be controlled by astigmatism light display during 6H.
[0825]Drawing 177 (b) shows the displaying condition after [Drawing 177 (a) to] 1H. One pixel row of write-in selected pixel rows 871a are shifted. In Drawing 177 (a), the blocks of the non display regions 312 are 1981b, 1918d, 1981f, 1981h, and 1981j. In Drawing 177 (b), the block of the non display regions 312 is 1981a, 1918b, 1981e, 1981g, and 1981i. That is, it is reversed except block 1981b including the write-in pixel row 871a selected with Drawing 177 (a) and (b) (the non display regions 312 and the image display region 311 are reversed).
[0826]A selected picture element line may not be limited to one pixel row, and the number of them may be [two or more]. For example, as drawing 34, drawing 35, drawing 89, etc. explained, it is combinable with a block drive of a method and Drawing 177 or a reverse-bias-voltage drive of Drawing 173 etc. which chooses two or more pixel rows.
[0827]Although TFT11d for switching of the selected picture element line was made into the OFF state and EL element 15 carried out to not making the light switch on in Drawing 177, in current mirror composition, the source signal line 18 and EL element 15 are not connected like drawing 8. Therefore, a selected picture element line is also good also as a displaying condition. however, the selected picture element line having been under program, it having presupposed that reversal with the non display regions 312 and the image display region 311 is performed 1H cycle in Drawing 177 with preferred controlling in the astigmatism light state, since the picture of the period was seen and flagged, but. It may be not the thing limited to this but 2H, or may be more than it. Light control may be performed comparatively at random. The reverse bias voltage Vm may be impressed to the block of astigmatism light with a natural thing.
[0828]It is not necessary to perform simultaneously control with the non display regions 312 and the image display region 311 by the pixel of RGB, and light control may be changed by R, G, and B. Also in FSC (frame sequential control), this is contained.
[0829]Although Drawing 177 presupposed that on-off control is performed for every block, it is not limited to this. For example, as shown in Drawing 178, they are two blocks (for example, the blocks 1981b and 1981c are made into the non display regions 312 in Drawing 178 (a).). let the blocks 1981d and 1981e be the image display regions 311 -- **** -- it may control. After 1H, as shown in Drawing 178 (b), light control may be performed. With Drawing 178 (a) and (b), it shifts 1 block at a time, and light control is performed. In Drawing 177 and Drawing 178, in order to illustrate easily, the number of the blocks 1981 is

lessened dramatically. Also in other examples, the above matter is the same.
[0830]Drawing 179 shows the method of forming lightness distribution in the display screen 21 by the light control of a block. In order to explain easily, Drawing 179 (a) is changed into theH [1st] state, and Drawing 179 (b) is explained that it is after 1H next to Drawing 179 (a). Of course, Drawing 179 (a) and (b) should just show in the state to which the prescribed period got used.
[0831]Gaussian distribution is illustrated in order to constitute lightness distribution. That is, it is the technique of making it bright visually and reducing power consumption by making the center section of the display screen bright and making a periphery dark. In this invention, by the abnormal conditions of a video signal, the longitudinal direction of a screen changes the data itself and forms lightness distribution. For example, the line memory of one pixel row is carried and the coefficient required for an operation is made to hold in this memory. For example, if the end of a screen is 50% as compared with a center section, the coefficient equivalent to 50% will be made to hold. The coefficient is made to hold hereafter, so that a center section may be 100% in a line memory, and so that Gaussian distribution may be satisfied. The impressed image data calculates with the coefficient of this line memory, and the calculated result is impressed to each source signal line.
[0832]If a pixel configuration is carried out so that the non display regions 312 can be turned on and off also to the lengthwise direction of a screen, the data itself will be changed by the abnormal conditions of a video signal, therefore it will become unnecessary for the longitudinal direction of a screen to form lightness distribution. For example, what is necessary is just to form a signal wire so that the on-off control of the TFT11d for switching of one pixel row can be carried out. That is, what is necessary is just to enable it to control TFT11d for switching by a display screen to matrix form.
[0833]Gaussian distribution is one example. That is, the distribution state of the luminosity which makes bright the neighborhood of a center section of the display screen 21 is generated. Therefore, it may be the lightness distribution of the shape of a sine curve instead of what is limited to Gaussian distribution, or may be the lightness distribution of conical shape. Since this invention controls TFT11d for switching, etc. and lightness distribution is generated, it is not limited to making the center section of the display screen 21 bright. For example, the center section of the display screen may be in the darkest state, and in the brightest state may be sufficient as the upper part of a display screen. It is easily realizable when these lightness distribution states also control TFT11d for switching, etc. It is because it is only realizable by making the control timing of the gate signal line 17b, and ON time adjust (change).
[0834]In accordance with the kind of picture, a user can change the distribution state of a luminosity freely or automatically. For example, a partialness display position can be especially displayed brightly at the time of a partial display. The color of arbitrary display portions can be changed easily, or it can display so that only a required portion may look bright outdoors.
[0835]A luminosity is not limited to what the three primary colors of R, G, and B are changed to the same position, and are generated for simultaneous (white moves). For example, the maximum luminance position of only R can also be moved. As mentioned above, the love scene in the display screen 21 can be generated by changing the maximum luminance (minimum luminance) position of each color.
[0836]The on-off control of the block 1981 realizes formation of distribution of the luminosity in the sliding direction of the display screen 21. That is, the number of times of OFF of the block 1981 of the center section of the display screen is lessened, and a display screen top or the bottom increases the number of times of OFF. A display screen becomes dark and becomes so bright that it decreases, so that there is much number of times of OFF. Gaussian distribution can be formed in the sliding direction of a display screen by controlling this turning on and off. Therefore, the longitudinal direction of a screen adjusts a luminosity with the operation (or amplitude value may be modulated by analog modulation) of picture image data, etc. (control), and the sliding direction of a display screen performs lightness adjustment (control) of a display screen by the on-off control of the block 1981.
[0837]In Drawing 179 etc., although it presupposed that lightness distribution is formed by the on-off control of the block 1981, it is not limited to this. It cannot be overemphasized not only the block 1981 but by carrying out on-off control for every pixel row that lightness distribution can be formed. Carrying out on-off control for two or more pixel line of every can also be realized. That is, on-off control of saying [carrying out on-off control with the block 1981] is only carried out as a meeting of two or more pixel rows. Therefore, Drawing 179 shows one example to which the technical scope of this invention was limited.
[0838]The non display regions 312 in Drawing 179 (a) are the blocks 1981b, 1981d, 1981h, and 1981j. The non display regions 312 in Drawing 179 (b) are the blocks 1981a, 1981c, 1981i, and 1981k. Therefore, Drawing 179 (a) and (b) has turned on the blocks 1981e, 1981f, and 1981g of a center section. Therefore, a

center section becomes bright.
[0839]On the other hand, although the blocks 1981a, 1981c, 1981i, and 1981k are the image display regions 311 in Drawing 179 (a), they are the non display regions 312 conversely in Drawing 179 (b). Therefore, the vertical section of a display image becomes dark.
[0840]From the above thing, lightness distribution can be formed in a display image by carrying out on-off control every block 1981. In Drawing 179, although Drawing 179 (a) and (b) has turned on the blocks 1981e, 1981f, and 1981g of a center section, by controlling changing into an astigmatism light state etc. by the following 1H, control of a luminosity can be realized freely and generating of a flicker can also be controlled.

[0841]In Drawing 179, all the width of the block 1981 was the same. However, visually, the center section of the display screen 21 may be made fine, and a periphery may be made rude, for example, as shown in Drawing 180, it carries out. This is because the resolution by human being's vision of the center section of the screen is high.
[0842]In Drawing 180, on-off control performs Drawing 180 (a) and (b) by turns. And in the blocks 1981f-1981n of the center section of the display screen 21, on-off control is performed by a fine block unit (one unit), the upper and lower sides of said center section perform on-off control by 2 block units, and the upper and lower sides of a display screen perform on-off control by 3 block units. OFF control of the write-in pixel row 871a is performed by the method explained with Drawing 177, and let it be the non display regions 312.
[0843]Although Drawing 180 realized the display which performed on-off control in the center section of the display screen by changing the width of the lighting block 1981, and was united visually, Drawing 181 realizes the Gaussian distribution of a display screen by controlling the number of times made to turn on and off in a cycle of two or more units. Drawing 181 forms the lightness distribution of a display screen six cycles (a figure -- 181 -- (-- a --) -- -> -- (-- b --) -- -> -- (-- c --) -- -> -- (-- d --) -- -> -- (e) ->(f) ->(a) ->(b) ->(c) ->(d) ->(e) ->(f) -> (a)). Of course, they may be not the thing limited to six cycles but two cycles, and eight cycles or more. What is necessary is just to synchronize the unit of a cycle with 1H, 1F, or other clocks. Also in Drawing 181, a video signal etc. perform the Gaussian distribution to the longitudinal direction of a display screen. Since this explains with Drawing 177 etc., it is omitted. The above matter is applied to other this inventions.
[0844]As shown in Drawing 181, with Drawing 181 (b) and (e), the center section of the display screen is made to generate the image display region 311, and Drawing 181 (c) and (f) is generating many image display regions near the center of a display screen. By controlling in this way, the center section of the display screen becomes bright. Therefore, good Gaussian distribution can be generated.
[0845]Drawing 182 controls generating of a flicker by not generating Gaussian distribution and changing the position of the lighting block 1981 in two or more periods. In Drawing 182 (a), the non display regions 312 are generated every 2 blocks, and the non display regions 312 are generated every 3 blocks in Drawing 182 of the following block (b). In Drawing 182 of the following block (c), the non display regions 312 are generated every 4 blocks. As mentioned above, generating of a flicker can be controlled by changing the position of the non display regions 312 or the image display region 311 with two or more cycles. Gaussian distribution can also be generated by combining the method explained with Drawing 180 and Drawing 181.
[0846]The above example changes a lighting position with 1981 units of blocks so that it may illustrate to Drawing 183. However, this invention is not limited to this. For example, it may change 1/2 block of lighting positions at a time so that it may illustrate to Drawing 184. That is, although it mainly explained carrying out on-off control of the above example by a block unit, it is not limited to this. It is because generating of Gaussian distribution and control of a flicker are realizable even if they are not 1981 units of blocks. What is necessary is just to carry out astigmatism light control per 1 pixel row, as explained above. Of course, what is necessary is just to carry out astigmatism light control or light control per two or more pixel line.
[0847]On-off processing may be carried out not by the thing limited to a pixel row but by a pixel row, and on-off processing may be carried out by both the pixel row and a pixel row. Pixel rows turned on and off are not limited to carrying out sequential operation, and may carry out random processing. By carrying out on-off control of the pixel row (pixel row) at random, the display screen 21 can be carried out that it is hard to be visible, or a flicker can also be generated. A specified pixel line (pixel row) can also always be made into the non display regions 312. Flashing of the screen can be carried out by giving an on-off indication (the non display regions 312 and the image display region 311 are repeated by turns) of the whole screen or the part with a low frame rate. These are applicable as the scramble processing or special effect processing of a picture.
[0848]However, when the above displaying condition controls by 1981 units of blocks, it cannot be

overemphasized that circuitry becomes easy and becomes easy [panel structure and a pixel configuration].

[0849]A picture is displayed by scanning the image display region 311 downward from on the display screen 21 so that it may illustrate to Drawing 185 ((a) ->(b) ->(c) ->(d) ->(e) ->(a) ->(b) -> (c) ->). At this time, lightness distribution (Gaussian distribution etc.) is realizable for the sliding direction of a display screen by controlling a scanning clock.

[0850]In Drawing 185, according to the displaying condition of (c), when the image display region 311 is scanned, the scan speed of the image display region 311 is made late. When the image display region 311 is scanned by the portions of (a) and (e), the scan speed of the image display region 311 is made quick. When the image display region 311 is scanned by the portions of (b) and (d), the scan speed of the image display region 311 is made into a middle speed of (a) and (c). A scan speed is realizable by controlling CLK* impressed to the shift register 22 of the gate driver 12 explained by drawing 10 etc. It is realizable by controlling the light control line 1791 explained with Drawing 155 etc.

[0851]As mentioned above, by controlling the image display region 311, the center section of the display screen 21 serves as high-intensity most, and the up-and-down portion of a screen becomes the darkest. Therefore, Gaussian distribution etc. can be formed in the sliding direction of the display screen 21. Of course, it may control in the direction of a pixel row, and Gaussian distribution etc. may be formed in the longitudinal direction of a screen. Data processing of a video signal is also realizable.

[0852]Although it presupposed that luminance distribution, such as Gaussian distribution, is formed in a display screen by changing the scanning speed of the image display region 311 in a screen position in Drawing 185, this technical idea is not limited to an EL display. For example, it is clear that it is applicable also with LED display equipment. It is not limited to a self-luminescence type display panel (display). For example, a liquid crystal display is also applicable.

[0853]In a liquid crystal display, a back light is improved and it realizes. That by which two or more luminous regions of stripe shape have been arranged in accordance with the direction of a pixel row is used for a back light. For example, the white EL element of stripe shape uses what was formed at least ten or more in accordance with the direction of a pixel row. What is necessary is just to turn on the light emitting device of this stripe shape sequentially from the top. That is, if the lighting times of stripe shape EL element 15 applicable to the center section of the display screen 21 are lengthened when making the EL element of stripe shape turn on, the luminescent state of a back light can be changed into the state of Drawing 185.

[0854]Therefore, in a liquid crystal display, for the very thing itself, a lighted indication state cannot be carried out, as shown in Drawing 185, but the image display explained with Drawing 185 is realizable by making the lighting field of a back light into a scanning state. It cannot be overemphasized that the above matter is applicable also in Drawing 177, Drawing 188 - Drawing 190, etc.

[0855]Drawing 186 is illustrating the driving waveform of the gate signal line 17a. The cycle of MCLK is set to 1H (one horizontal scanning period) in order to explain easily. However, it is not limited to this. Supple control is realizable by using a clock more nearly high-speed than 1H.

[0856]The portion shown by 'a' of Drawing 186 corresponds to the displaying condition of Drawing 185 (a). Similarly the portion shown by 'b' of Drawing 186 corresponds to the displaying condition of Drawing 185 (b), and the portion shown by 'c' of Drawing 186 corresponds to the displaying condition of Drawing 185 (c). The portion shown by 'd' of Drawing 186 corresponds to the displaying condition of Drawing 185 (d), and the portion shown by 'e' of Drawing 186 corresponds to the displaying condition of Drawing 185 (e).

[0857]A pixel configuration explains by illustrating the composition of drawing 6. Therefore, when ON state voltage Vgl is impressed to the gate signal line 17a, an applicable pixel row is chosen. However, the example of this invention is not limited to the pixel configuration of drawing 6, and can be applied also to the pixel configuration of voltage programs, such as current mirror composition, such as drawing 8, drawing 75, and drawing 76.

[0858]A pixel row is shifted to the portions of 'a' and 'e' with a 1H piece clock so that it may illustrate to Drawing 186. A pixel row is shifted to the portions of 'b' and 'd' with a 2H piece clock. A pixel row is shifted to the portion of 'c' with a 3H piece clock. Therefore, the portion of 'c' has a late shift action of 3 times and a pixel row as compared with the portion of 'a'. That is, the portion of 'c' becomes bright 3 times as compared with the portion of 'a'. Therefore, the center section of the screen becomes the brightest and a vertical section can be made the darkest.

[0859]In Drawing 186, data transfer of the shift register 22 was used as three clocks in the center section of the display screen. Data transfer of the shift register 22 was used as one clock in the vertical section of a display screen. Data transfer of the shift register 22 was used as two clocks in the vertical section and

center section of the display screen. However, as shown in Drawing 186, the boundary line of a change is distinctly displayed that the change of a clock is a three-stage with the difference of a luminosity. Therefore, while making the difference of a data transfer clock small in practice so that a boundary line cannot be seen, it is preferred to make various the changing clock number. That is, Drawing 186 is a figure for explanation.

[0860]For example, in the center section of the display screen, data transfer of the shift register 22 is used as five clocks, use data transfer of the shift register 22 as three clocks in the vertical section of a display screen, and let data transfer of the shift register 22 be four clocks in the vertical section and center section of the display screen.

[0861]Make a display screen more than the field of 9 division, and The 1st field from a display screen, the 2nd field, the 3rd field, ... If it is considered as the 9th field, use data transfer of the shift register 22 as 15 clocks for the 5th field of a center section, and let data transfer of the shift register 22 be 11 clocks for the 1st field and the 9th field. Let data transfer of the shift register 22 be 12 clocks for the 2nd field and the 8th field. Let data transfer of the shift register 22 be 13 clocks for the 3rd field and the 7th field. Let data transfer of the shift register 22 be 14 clocks for the 4th field and the 6th field. As mentioned above, if a display screen is divided and on-off control is carried out to optimum, respectively, the boundary line of a luminosity is not conspicuous.

[0862]The method of Drawing 187 is also effective to making it not seen [the boundary line of the luminosity of a display screen]. In Drawing 187, the signal wave form of the gate signal line 17a of the center area of the display screen 21 is illustrated.

[0863]As shown in Drawing 187, the shift start timing of three clocks to a display position is changed in each field (frame) (F). In order for Drawing 187 to explain easily, in 1F to 4F, it has shifted one clock of starting positions at a time. Although it does not shift one clock at a time for every F and being actually shifted by one clock by certain F, it processes not shifting etc. in other F. The number of times which shifts three clocks is changed the whole F.

[0864]For example, the starting position of three clocks of the center section of the display screen presupposes that the 1st F is started from a pixel row (90) and (90 pixel-row eye), and it makes the range to which a shift register is transmitted with three clocks 20 pixel rows. The starting position of three clocks of the center section of the display screen presupposes that the 2nd F is started from a pixel row (92), and it makes the range to which a shift register is transmitted with three clocks 16 pixel rows. The starting position of three clocks of the center section of the display screen presupposes that the 3rd F is started from a pixel row (94), and it makes the range to which a shift register is transmitted with three clocks 12 pixel rows. The starting position of three clocks of the center section of the display screen presupposes that the 4th F is started from a pixel row (96), and it makes the range to which a shift register is transmitted with three clocks eight pixel rows. It can be made hard to be are the brightest in a center section and conspicuous [from the display luminance of the upper part of a display screen / in the boundary line which changes to the display luminance of this center section] by processing as mentioned above.

[0865]The starting position of a shift processes to looped shape. Drawing 187 -- 1F->2F->3F->4F->1F->2F -- it repeats with .... As it is not limited to this although the center section of the display screen presupposes that a pixel row is shifted with 3 clock periods, and Drawing 186 explained it in Drawing 187, it cannot be overemphasized that a clock number and a viewing area are adjusted so that luminance distribution may change smoothly.

[0866]It cannot be overemphasized by combining Drawing 186 and Drawing 187 that lightness distribution processing of a screen display is not conspicuous, and a good display can be realized further.

[0867]Although the drive method explained with Drawing 186 and Drawing 187 formed luminance distribution in the display screen 21 intentionally, this technical concept is applicable to other image display.

[0868]Drawing 188 forms two luminosity portions in the display screen 21 (display). In Drawing 188, displaying the image display region 311a more brightly than the image display region 311b is shown. In Drawing 188 (a), the image display region 311a of the memo 1 is made brighter than other image display regions 311b. Displaying the image display region 311a more brightly than the image display region 311b can comprise easily a method explained with Drawing 185 etc. Since what is necessary is just to control the number of times which chooses the viewing area of each part, it is easily realizable by other methods.

[0869]In Drawing 188, user-friendliness of the display is made good by displaying the field which a user chooses brightly (or darkly). Of course, it is also preferred to change the color of the selected image display region 311. As for the method of presentation of Drawing 188, applying to a menu selection screen

etc. is preferred. It is because a screen display can be changed by a user's operation and operativity improves. Control of a microcomputer etc. may constitute so that it may be in the screen-display state of Drawing 188 automatically. Outdoor daylight is strong outdoors, and since a display image disappears, it may control to turn on only a required portion strongly especially (image display region 311a). For example, the luminosity of outdoor daylight is detected, and when the strength of the detected outdoor daylight is beyond constant value, it is a case where the user pushed the electric power switch and the display screen 21 is displayed etc.

[0870]The image display region 311a turned on strongly may be established in two or more places of the display screen 21, or it may be made to blink so that it may illustrate to Drawing 189 (a). It is making the image display region 311a turn on and off in a 0.5-second cycle, or making low-intensity and high-intensity display by turns that it makes it blink in Drawing 189 (a).

[0871]Image display may be performed combining the high-intensity image display region 311a, the low-intensity image display region 311b, and the non display regions 312 so that it may illustrate to Drawing 189 (b).

[0872]Drawing 190 gives the scroll effect of the display screen 21. In Drawing 190 (a), it is considered as the high-intensity image display region 311a to the center section of the display screen 21, and Drawing 190 (b) is considering it as the high-intensity image display region 311a to near the lower end of the display screen 21.

[0873]It cannot be overemphasized that it is also possible to indicate the display screen 21 whole by low-intensity simultaneously. This invention adjusts the luminosity of the display screen 21 by making the current which controls the light control line 1791 or the gate signal line 17b, and flows into EL element 15 turn on and off (control). Therefore, since the image data outputted from the source driver 14 does not change, the contrast of a display image and a gamma curve have the feature also in not being based on the luminosity of a display image but constant value being maintained. Therefore, even if it indicates the display screen 21 whole by low-intensity simultaneously, a gradation characteristic is maintained as it is (for example, when indicating by 64 gradation, 64 gradation is maintained even if the luminosity of a display screen is set to one half).

[0874]In order to demonstrate the effect of making the display screen 21 whole into the low-intensity image display region 311b first (considering it as the low-intensity display), and rewriting a display screen so that it may illustrate to Drawing 190, From on the display screen 21, it uses down with the high-intensity image display region 311a (it is considered as the bright display). Therefore, the one display screen 21 is rewritten by performing the bright display to the arrow direction of Drawing 190. And between fixed time, if a bright display makes it continue, the display screen 21 whole will be made a low-intensity display from a viewpoint of low power consumption.

[0875]In an organic electroluminescence display panel, big electric power is needed by a white raster display. If the power supply circuit for these white raster displays is provided, a power supply circuit will become very large. On the other hand, in the usual character display, only the electric power of 1 / 5 - 1/3 of a white raster display is wasted. Therefore, it is economical to hold the output current of a power supply so that a white raster display can respond, or it is not preferred from a viewpoint of system size.

[0876]In order to cope with this technical problem, when displaying the pictures (for example, white raster display etc.) which have the electric power beyond constant value consumed, it constitutes from this invention so that the luminosity of a picture may be reduced and may be displayed. For example, when 100-mA current flows by a white raster, image data is processed so that it may become one half of 50-mA current. That is, when it asks for total of the data of an inputted image and total becomes beyond constant value, the value of image data is made small so that data processing may be performed to image data and it can display with the power to hold.

[0877]Of course, the luminosity of the display screen 21 whole can be reduced by performing astigmatism light control explained with not the thing limited to making the value of image data small but Drawing 155, Drawing 185, Drawing 189, etc. Of course, the luminosity of only a picture display part is reduced and it cannot be overemphasized that icon portions, such as an antenna display and a clock display, are also controllable to maintain the conventional luminosity (luminosity as it is).

[0878]By scanning the image display region 311 or the non display regions 312 to the sliding direction of a display screen, the above example explained noting that it formed a luminosity viewing area which performs image display or is different (display). However, this invention is not limited to this. For example, in Drawing 188 etc., if the number of times which chooses each portion of the display screen 21 is controlled, lightness distribution can be formed. That is, in Drawing 188, if it controls to choose the image display region 311b 25 times, and to choose the image display region 311a 50 times when the frame rate which

displays the display screen 21 is 60 Hz, the image display region 311a can be displayed in an image display region twice the luminosity of 311b. When similarly the frame rate which displays the display screen 21 in Drawing 190 (b) is 60 Hz, If it controls to choose the image display region 311b 25 times, to choose the image display region 311a 50 times, and not to choose the non display regions 312 at all, the image display region 311a can be displayed in an image display region twice the luminosity of 311b, and can make the non display regions of 312 a black display.

[0879]It cannot be overemphasized that the matter explained above is applicable also to the reverse-bias-voltage drive explained with the block drive or Drawing 173 explained with Drawing 172 etc. As for the number of the pixel row which constitutes each block, in a block drive, it is preferred to use the number expressing one character string. For example, if one character comprises 16x16 dots, 16 pixel rows will be considered as one block. If one character comprises 24x24 dots, 24 pixel rows will be considered as one block. Thus, the image display region 311 and the non display regions 312 are controllable for every line which displays a character by the dot number of the lengthwise direction which constitutes a character coinciding the block count.

[0880](Embodiment 10) Like the method of presentation of drawing 52, the method of presentation changed to every predetermined field (frame) can apply an odd number pixel row and an even number pixel row (two or more pixel line of every [or]) to a stereoscopic picture display device or a method. Hereafter, it explains, referring to Drawing 191 and Drawing 192 for the stereoscopic display device of this invention.

[0881]First, the method of presentation of this invention constitutes the image display region 311 and the non display regions 312 per pixel row (the direction of a pixel row) fundamentally. Therefore, to display like drawing 52, it is necessary to change every direction but, and this conversion is easy. It is because what is necessary is just to replace a row and column for the image data accumulated in the memory. If every direction is changed, it will be in the displaying condition of Drawing 191 (a1). That is, although the scanning direction of a display panel turns into an arrow direction shown in A, as a picture is shown in Drawing 191 (a1), a space top becomes a screen top and the bottom of space becomes the bottom of a screen. Therefore, it is visible to the user of a display panel as scanned downward from on a screen.

[0882]The display screen 21 of a display panel displays the picture of a right eye on an odd number pixel row (line) from the left, and displays the picture of a left eye on an even number pixel row (line). Image display is synchronized with the glasses 852 for observation which synchronize with a display panel. The glasses 852 for observation possess two liquid crystal panels which function as the shutter 851.

[0883]In the 1st field (the 1st frame), as shown in Drawing 191 (a1), the odd-numbered pixel row (in practice odd-numbered pixel row) serves as the image display region 311 from the left, and the even-numbered pixel row (in practice even-numbered pixel row) serves as the non display regions 312 from the left. Synchronizing with the displaying condition of Drawing 191 (a1), the shutter 851L for the left eyes of the glasses 852 for observation closes, and the shutter 851R for the right eyes of the glasses 852 for observation opens. Therefore, an observer is only a right eye and will look at the picture of Drawing 191 (a1).

[0884]As the 2nd next field (the 2nd frame) of the 1st field (the 1st frame) shows to Drawing 191 (a2), The even-numbered pixel row (in practice even-numbered pixel row) serves as the image display region 311 from the left, and the odd-numbered pixel row (in practice odd-numbered pixel row) serves as the non display regions 312 from the left. Synchronizing with the displaying condition of Drawing 191 (a2), the shutter 851R for the right eyes of the glasses 852 for observation closes, and the shutter 851L for the left eyes of the glasses 852 for observation opens. Therefore, an observer is only a left eye and will look at the picture of Drawing 191 (a2).

[0885]By repeating the above operation by turns, a stereoscopic picture display is realizable by glasses type the shutter 851 and image display state which an observer uses synchronizing, and making it visible to an observer by turns.

[0886]What is necessary is just to arrange the prism 861 to the optical display panel's outgoing radiation side, as illustrated to Drawing 192 in order to realize a stereoscopic picture display, without using the shutter 851. It arranges so that it may correspond to the image display region [in / for the A section of the prism 861 / a certain display timing] 311, and it arranges so that it may correspond to the non display regions [in / for the B section of the prism 861 / the above-mentioned display timing] 312. Thus, by arranging the prism 861, it can constitute so that it may be made for the picture of an odd number pixel row to enter into an observer's right eye and the picture of an even number pixel row may enter into an observer's left eye. Between the prism 861 and a display panel, optical coupling of the optical coupling material 862, such as ethylene glycol, is arranged and carried out.

[0887]Although the switching means 852 was used as glasses in Drawing 191, it is not limited to this. Which

thing may be used as long as the light which enters into an observer's right eye, and the light which enters into a left eye are controllable. For example, a goggles type thing is illustrated. That (head mount display) with which the switching means 852 and the display panel were united is illustrated. The shutter 851 may not be limited to a liquid crystal display panel, and may be mechanical like the shutter of a camera, and a turnable filter. The thing incorporating a polygon mirror, the shutter using PLZT, the shutter adapting electroluminescence, etc. are illustrated.

[0888]As mentioned above, a three dimentional display is realizable by using the method of presentation of drawing 52 for the display image of one display panel. It says that the device or method of Drawing 191 and Drawing 192 displays a picture which is different in two or more pixel line (sequence) of every, and an odd number pixel row (sequence) and every even number pixel row (sequence), and the use is not limited only to a three dimentional display. For example, it may use for the use of only piling up and displaying two pictures. It cannot be overemphasized that especially the thing for which the drive method of this invention is enforced using the EL display of this invention is effective.

[0889]Although the element which drives each pixel was set to TFT11, it is not limited to this. For example, with the combination of a thin-film diode (TFD), the pixel 16 can be constituted and the intermittent control action of the current sent through EL element 15 can be carried out by operating one terminal voltage level of this diode. In this composition, a cathode terminal and horizontal stripe shape are processed if needed (formation). In addition, it is the same also at switching elements, such as a barista and a thyristor.

[0890]For example, as long as it makes TFT for a drive in TFT11a for conversion of drawing 6 into an example, the bipolar transistor of N channel or P channel may be sufficient so that it may illustrate to Drawing 193 (a). The MOS transistor of N channel or P channel may be sufficient so that it may illustrate to Drawing 193 (b). A photo transistor or a photo-diode may be used, and a thyristor element etc. may be sufficient so that it may illustrate to Drawing 193 (d), so that it may illustrate to Drawing 193 (c). This means being applicable also to the switching element which constitutes other pixels.

[0891]The TFT element can use N either P channel or a channel. The position of EL element 15 is not limited to a position like drawing 6 or drawing 8. For example, Drawing 153 (a) extracts the connected state of TFT11a for conversion of drawing 6, and EL element 15. The composition of Drawing 153 (b) is also illustrated as this modification. The composition of Drawing 153 (c) which used TFT for a drive as N channel, and (d) is also illustrated. These matters are the same about the switching element which constitutes other pixels a [not only / TFT11/ not only] for conversion.

[0892]Although it is desirable to be formed by low-temperature polycrystal Si-TFT as for switching elements, such as TFT, the amorphous silicon TFT may be sufficient. It is more enough on the characteristic to form with amorphous silicon art, especially when the current sent through EL element 15 is below 1microA. A gate driver circuit, a source driver circuit, etc. may be formed with the element by amorphous silicon art.

[0893]It is not what is limited also for the composition of the gate drivers 12, such as drawing 10, drawing 55, drawing 56, and drawing 58, to this (drawing 10 is composition which carries out the shift action (serial processing) of the ST signals one by one synchronizing with a clock), For example, it may be a parallel input which determines the on-off state of each gate signal line at once (the one OFUFU logic of all the gate signal line is a part for the number of a controller or the gate signal line 17, the composition which are outputted at once and for which it opts, etc.).

[0894]Drawing 194 is a lineblock diagram of an organic electroluminescence module. Control IC101 and power supply IC102 are mounted in the printed circuit board 103. The printed circuit board 103 and the array substrate 49 are electrically connected by the flexible substrate 104. Power supply voltage, current, a control signal, and picture image data are supplied to the source driver 14 and the gate driver 12 of the array substrate 49 via this flexible substrate 104.

[0895]Under the present circumstances, the control signal of the gate driver 12 poses a problem. It is necessary to impress the control signal of the amplitude beyond 5V to the gate driver 12 at least. However, since the power supply voltage of control IC101 is 2.5V or 3.3V, it cannot impress a control signal to the gate driver 12 directly from control IC101.

[0896]This invention impresses the control signal of the gate driver 12 to this technical problem from power supply IC102 driven on high voltage. Since power supply IC102 also generates the operating voltage of the gate driver 12, though natural, the control signal of the optimal amplitude for the gate driver 12 can be generated.

[0897]In Drawing 195, the control signal of the gate driver 12 is generated in control IC101, and once the source driver 14 performs a level shift, it is being impressed by the gate driver 12. Since the driver

voltages of the source driver 14 are 5-8V, they can change the control signal of 3.3V amplitude outputted from control IC101 into 5V amplitude which can receive the gate driver 12.
[0898]Drawing 132 and Drawing 196 are explanatory views of the display module device of this invention. Drawing 196 shows the composition of having given the built-in display memory 151 in the source driver 14. Built-in display memory has the capacity of 8 color specification (1 bit of each color), 256 color specification (RG is a triplet and B is 2 bits), and 4096 color specification (RGB is 4 bits each). Since the driver controller with which it is these eight colors, 256 colors, or 4096 color specification, and has been arranged in the source driver 14 at the time of a still picture reads the image data of this built-in display memory 151, super-low power consumption is realizable. Of course, the built-in display memory 151 may be the multicolor display memory of 260,000 or more colors. The image data of the built-in display memory 151 may be used also at the time of an animation.
[0899]The image data of the built-in display memory 151 may carry out the memory of the data after performing an error diffusion process or dithering. By performing an error diffusion process, dithering, etc., 260,000 color specification data can be changed into 4096 colors etc., and capacity of the built-in display memory 151 can be further made small. The error diffusion controller 141 can perform error diffusion processes. After performing dithering, an error diffusion process may be performed further. The above matter is applied also to a reverse error diffusion process.
[0900]In Drawing 196 etc., although 14 was indicated to be a source driver, Power supply IC[not only a mere driver but] 102, the buffer circuit 154 (circuits, such as a shift register, are included), The various functions or circuits which process the input from a data conversion circuit, latch circuitry, a command decoder, a shift circuit, an address conversion circuit, and the built-in display memory 151, and output voltage or current to a source signal line are constituted. These matters are the same in other examples of this invention.
[0901]It cannot be overemphasized that the composition explained with Drawing 196 etc. is applicable to three-side free composition or other composition, a drive method, etc. which are explained by drawing 12 - drawing 16, drawing 18, drawing 20, drawing 21, etc.
[0902]Drawing 197 shows the example of composition which used the protective cover for protecting EL element 15 from humidity as the closure lid 41, and may be used also [protective covers /, such as a cellular phone,]. A protective cover is a transparent plate arranged in order to protect the front face of a display panel. Or in the reflection type liquid crystal display panel, the front light serves as a protective cover. And the circular light board 74 is attached to the closure lid 41. The circular light board 74 may apply resin to a thin film or the closure lid 41, and may form it by extending this resin.
[0903]And the array substrate 49 of the EL element is attached to the cases 193, such as a cellular phone (the EL display panel is attached). The gate driver 12 (or source driver 14) is arranged in the closure lid 41. The gate driver 12 (or source driver 14) is also protected by the closure lid 41. By forming as mentioned above (Elements of the Invention), a protective cover can be omitted and thickness as [whole] a display panel module can be made thin.
[0904]As drawing 2 also explained, the organic EL panel needs to form the reflection film 46 as a cathode terminal (or anode electrode). This electrode is formed with aluminum etc. Therefore, reflectance is as good as not less than 85%.
[0905]Drawing 198 shows the cellular phone constituted so that this reflection film 46 could be used as a mirror. It is used so that it may illustrate to Drawing 199 in the state of anticipated use (or refer to Drawing 200). When using the display panel 2046 as a mirror, the display panel 2046 is turned focusing on the fulcrum (not shown) of the right or the left, and the rear-face mirror 2045 is used.
[0906]However, the reflection film formed in the rear face of an EL display panel is used for the above example as a mirror. Therefore, the object used as a mirror may not be limited to a cellular phone, and television, a monitor, and PDA may be sufficient as it. A mirror is formed in the rear face of a display panel. Therefore, not the thing limited to a cathode but the composition which formed the mirror in the rear face of a display panel separately may be used. For example, in a reflection type liquid crystal display panel, since the rear face is not used, aluminum or silver may be vapor-deposited at this rear face, and a mirror may be formed in it. In this case, in order to prevent aluminum or silver from corroding, it is preferred to form inorganic thin films, such as SiO_2, in the surface. UV resin may also be protected.
[0907]In Drawing 198, 2041 is a speaker the sound which received is made to be heard, and 2044 is a microphone for inputting a user's sound. As drawing 44 explained, it is preferred to arrange the display mode changeover switch 465. It is preferred to form the changeover switch which realizes the function which changes the luminosity of the screen explained by drawing 43 etc. (arrangement).
[0908]A frame rate is related to the power consumption of a panel module. That is, if a frame rate is made

high, power consumption will increase proportionally mostly. The cellular phone needs to aim at reduction of power consumption from viewpoints of lengthening standby time. On the other hand, in order to increase a foreground color (a gradation number is increased), drive frequency of the source driver 14 etc. must be made high. However, it is difficult to increase power consumption from the problem of power consumption.
[0909]Generally, priority is given to low power consumption over display color numbers in information display devices, such as a cellular phone. Power consumption increases from the reasons of the clock frequency of the circuit to which display color numbers are made to increase becoming high, or change of a voltage (current) waveform impressed to an EL element increasing. Therefore, display color numbers can seldom be increased. To this technical problem, this invention performs an error diffusion process or dithering for image data, and displays a picture.
[0910]Although not illustrated in the cellular phone of this invention explained with Drawing 199, the back side of the case is equipped with the CCD camera. The picture and data which were photoed with the CCD camera can be displayed immediately at the display screen 21 of a display panel. The image data of a CCD camera can change 24 bits (16,700,000 colors), 18 bits (260,000 colors), 16 bits (65,000 colors), 12 bits (4096 colors), and 8 bits (256 colors) by keystroke.
[0911]When an indicative data is 12 bits or more, it displays by performing an error diffusion process. That is, when the image data from a CCD camera is more than the capacity of the built-in display memory 151, an error diffusion process etc. are carried out, and image processing is performed so that below the capacity of the built-in display memory 151 may become about display color numbers.
[0912]Now, it explains providing the built-in display memory 151 of one screen by 4096 colors (4 bits each of RGB) in the source driver 14. When the image data sent from the module outside is 4096 colors, it is stored in the built-in display memory 151 of the direct source driver 14, image data is read from this built-in display memory 151, and a picture is displayed on the display screen 21.
[0913]When image data is 260,000 colors (G:6 bits, R, B: a total of 16 bits which is 5 bits each), as shown in Drawing 132 and Drawing 196, it is once stored in the operation memory 152 of the error diffusion controller 141, and error diffusion or dithering is performed simultaneously in the arithmetic circuit 153. 16-bit image data is changed into 12 bits which is the number of bits of the built-in display memory 151 by this error diffusion process, and it is transmitted to the source driver 14. The source driver 14 outputs the image data of 4 bits each (4096 colors) of RGB, and displays a picture on the display screen 21.
[0914]In the composition of Drawing 132, etc., an error diffusion process or a dither disposal method may be changed for every field or frame using Vertical Synchronizing signal VD (changing a disposal method with Vertical Synchronizing signal VD). For example, in dithering, a half-tone type is used by the following frame [2nd] at the 1st frame using a Bayer type. Thus, dithering is changed for every frame and the effect that the dot unevenness accompanying an error diffusion process etc. becomes difficult to be conspicuous by making it change is demonstrated.
[0915]Processing coefficients, such as an error diffusion process, may be changed by the 1st frame and the 2nd frame. An error diffusion process may be carried out by the 1st frame, dithering may be carried out by the 2nd frame, and various processings, such as carrying out an error diffusion process by the 3rd [further] frame, may be combined. A random number generation circuit may be provided and the disposal method which processes for every frame with the value of a random number may be chosen.
[0916]If information, including a frame rate etc., is indicated to the format transmitted, a frame rate etc. can be automatically changed by decoding or detecting this indicated data. In the case of that the picture transmitted indicates an animation or a still picture, especially an animation, it is preferred to indicate the number of tops per second of an animation. It is preferred to indicate the machine type number of a cellular phone to a transmission packet. Although this specification explains as a transmission packet, it is not necessary to be a packet, and any may be sufficient as long as the information, including display color numbers, a frame rate, etc., explained with Drawing 201 etc. into the data transmitted or sent is indicated.
[0917]Drawing 202 shows the transmission format sent to the cellular phone of this invention, etc. With transmission, the both sides of the data to receive and the data to transmit are included. That is, it is because a cellular phone may transmit the picture photoed with the CCD camera of attachment in the sound or cellular phone from a receiver to other cellular phones. Therefore, the matter relevant to the transmission format etc. which are explained with Drawing 201 etc. is applied to the both sides of transmission and reception.
[0918]In the cellular phone of this invention, etc., data is digitized and is transmitted by packet format. As Drawing 202 has indicated, the inside of a frame consists of flag part (F), address part (A), control section (C), and information bureau (I) and frame check sequence (FCS). The format of a control section (C) takes information transfer (I frame), surveillance (S frame), and three forms of an off duty item system (U frame),

as shown in Drawing 203.
[0919]First, information transfer format will be the form of the control field used when transmitting information (data), and if a part of non-number nature form is removed, information transfer format will be the only form of having a data field. The frame by this form is called data frame (I frame).
[0920]Supervisory format is a form used in order to perform the supervisor control function of a data link, i.e., the confirmation of receipt of a data frame, request sending of a data frame, etc. The frame by this form is called supervisory frame (S frame).
[0921]Next, it is the form of the control field used in order that off duty item system form may carry out other data ring control facilities, and the frame by this form is called unnumbered frame (U frame).
[0922]A terminal and a net manage the data frame transmitted and received by send-sequence-number N (S) and receive-sequence-number N (R). N (S) and N (R) comprised a triplet, eight to 0-7 was used as a circulation number, and the next of 7 has taken the modulus composition from which it is set to 0. Therefore, the modulus in this case is 8 and the frame number which can carry out continuous transmission without receiving a response frame is 7.
[0923]The 8-bit data in which the 8-bit data in which color number data is shown, and a frame rate are shown is indicated in a data area. These examples are shown in Drawing 201 (a) and (b). It is preferred to indicate distinction of a still picture and an animation to the color number of a foreground color. It is desirable to indicate the kind name of a cellular phone, the contents (natural drawings, such as a person, menu screen) of the image data transmitted and received, etc. to the packet of Drawing 202. The model which received data decodes data, and when it has been recognized to be own (applicable machine type number) data, it changes a foreground color, a frame rate, etc. automatically according to the indicated contents. It may constitute so that the indicated contents may be displayed on the display screen 21 of a display. A user operates a key etc., seeing the description content (a foreground color, a recommendation frame rate) of the display screen 21, and should just change into the optimal displaying condition by a manual.
[0924]As an example, with Drawing 201 (b), although numerical 3 has given and indicated frame rate 80Hz and an example, it is not limited to this, and it may show fixed ranges, such as 40-60 Hz. The model of cellular phone, etc. may be indicated to a data area. It is because the necessity of performances etc. differing depending on the model and changing a frame rate is also generated. Pictures are comics, it is advertisement (CM), or it is also preferred to indicate thing information. Audience fee gold and information, including packet length etc., may be indicated to a packet. It is because it can be judged whether a user checks audience fee gold and receives information. It is preferred to also indicate the data of whether image data is carried out in the error diffusion process.
[0925]What is necessary is just to indicate information, including an image processing method, machine type numbers (the kind of classification, such as an error diffusion process and dithering, and weighting function, the data, the coefficient of gamma, etc.), etc., to the format transmitted. If image data indicates the information on the resolution, MPEG data, BITMAP data, etc. again in the data photoed by CCD, and JPEG data, The auto-receipt cellular phone [data / decode, or detect and] based on this, etc. can be changed now into the optimal state.
[0926]Of course, in the case of that the picture transmitted indicates an animation or a still picture, especially an animation, it is preferred to indicate the number of tops per second of an animation. It is preferred to also indicate information, including the number of reproduction tops / second recommended with a receiving terminal.
[0927]The above matter is the same even when a transmission packet is transmission. Although this specification explains as a transmission packet, it is not necessary to be a packet. That is, any may be sufficient as long as the information explained with Drawing 201 etc. into the data transmitted or sent is indicated.
[0928]It is preferred to add again the function to perform an error diffusion process to the error diffusion process controller 141, after performing a reverse error diffusion process to the data which error processing was carried out and has been sent and returning to source data. The existence of the error diffusion process is put on the packet data of Drawing 202. Data required for reverse error diffusion processes, such as a disposal method of error diffusion (methods, such as a dither, are also included) and form, is also carried.
[0929]A reverse error diffusion process is carried out in the process of an error diffusion process because amendment of a gamma curve is also realizable. The transmitted data when gamma curves, such as an EL display which received data, and the sent gamma curve are not adapted may be image data which had error diffusion etc. already processed. In order to cope with this situation, a reverse error diffusion process is

carried out, it changes into source data, and the influence of gamma curve amendment is kept from coming out. Then, the EL display etc. which were received perform an error diffusion process, and an error diffusion process etc. are carried out so that it may be made the optimal gamma curve for a receiving display panel and may become the optimal error diffusion process.

[0930]What is necessary is to arrange a user button to devices, such as a cellular phone, and just to change a foreground color etc. using a button etc. to change a frame rate by a foreground color.

[0931]Drawing 199 is a top view of the cellular phone as an example of information terminal equipment. The antenna 191, the ten key 192, etc. are attached to the case 193. 194 is a foreground-color change key or power supply turning on and off, and a frame rate change key.

[0932]Internal circuit blocks, such as a cellular phone, are shown in Drawing 204. A circuit mainly comprises a block of the block of the up converter 205 and the down converter 204, the block of the duplexer 201, the LO buffer 203, etc.

[0933]If the key 194 is pressed down once, a foreground color will press down the same key 194 following 8 color modes and a foreground color will press down the same key 194 further 256 color modes, a foreground color may also construct a sequence so that it may become 4096 color modes. Whenever it presses down a key, let it be a toggle switch from which foreground-color mode changes. The change key to a foreground color may be provided separately. In this case, the key 194 is set to three (above).

[0934]Other mechanical switches, such as a slide switch besides a push switch, may be sufficient as the key 194, and it may change by speech recognition etc. For example, by carrying out voice input of the 4096 colors to carrying out voice input to a receiver, for example, "a high-definition display", "256 color modes" or "low foreground-color mode", and a receiver, it constitutes so that the color displayed on the display screen 21 of a display panel may change. This is easily realizable by adopting the present speech recognition technology.

[0935]The switch which changes electrically may be used for the change of a foreground color, and the touch panel chosen by touching the menu displayed on the display screen 21 of a display panel may be sufficient as it. It may constitute so that it may change or change by rotation or a direction like a click ball by the number of times which presses down a switch.

[0936]Although 194 considered it as the foreground-color change key, it is good also as a key etc. which change a frame rate. It is good also as a key etc. which change an animation and a still picture. Two or more requirements, such as a frame rate, may be simultaneously changed to an animation and a still picture. If it continues pressing down, it may constitute so that a frame rate may change gradually (continuously). In this case, it is realizable by making resistance R into a variable resistor, or making it into electronic volume among the capacitor C which constitutes an oscillator, and the resistance R. A capacitor is realizable by considering it as a trimmer capacitor. Two or more capacitors are formed in the semiconductor chip, one or more capacitors may be chosen, and these may be realized by connecting in parallel in circuit.

[0937]The technical idea of changing a frame rate by a foreground color etc. is not limited to a cellular phone, and can be widely applied to the apparatus which has display screens, such as a palmtop computer, a notebook computer, a desktop PC, watch. It is applicable also to not the thing limited to a liquid crystal display but a liquid crystal display panel, an organic electroluminescence display panel, a TFT panel, the PLZT panel, and CRT.

[0938]In Drawing 198, 2043 is a function switch (FSW). FSW2043 is arranged at the position pressed down with a digitus minimus and the third finger. FSW2043a and 2043b are arranged at right and left. This is because it constituted so that it could realize being pressed down with a right digitus minimus, being pressed down with the third finger and a left digitus minimus, and the third finger. FSW may be arranged at the rear face of the case 193.

[0939]The user is made to be changed by command setting out FSW2043 of a left hand is validated [whether FSW2043 for right hands is validated, or]. That is, if a user does setting out which validates the object for right-hand side by a menu screen, FSW2043 for right hands will become effective and FSW2043 of a left hand will become invalid. On the contrary, if a user does setting out which validates the object for left-hand side by a menu screen, FSW2043 for left hands will become effective and FSW2043 of a right hand will become invalid.

[0940]When FSW2043 is not pushed so that it may illustrate to Drawing 205 (a), the ten key 192 serves as a number input key. As shown in Drawing 205 (b), if FSW2043a is pushed, it will become hiragana input mode. this time -- "**, **, and ** -- ** -- the character of the top of -- and" is specified. "**" is first chosen in this state. Next, if FSW2043b is also pressed down, it will be in the input state of five characters containing the character string pressed down previously. A character will be inputted if a specific key is

pressed down in this state. Therefore, a Japanese input is easily realizable by combining FSW2043 and the ten key 192. If only FSW2043b is pressed down so that it may illustrate to Drawing 205 (d), it will become an English character input mode.
[0941]As mentioned above, various character inputs become possible easily by arranging FSW2043 other than the ten key 192.
[0942](Embodiment 11) The embodiment which adopted the EL display panel, EL display, or drive method of this invention is described further, referring to drawings.
[0943]Drawing 206 is a sectional view of the viewfinder in an embodiment of the invention. However, in order to explain easily, it is drawing typically. There are also a part expanded or reduced in part and an abridged part. For example, eyepiece covering is omitted in Drawing 206. The above thing corresponds also in other drawings.
[0944]The rear face of the body 451 is made a dark color or black. This is for the stray light emitted from the display panel 82 to carry out scattered reflection by the inner surface of the body 451, and to prevent the fall of display contrast. The lambda/4 boards 50 (phase plate etc.), the polarizing plate 54, etc. are arranged at the optical display panel's outgoing radiation side. Drawing 2 also explains this.
[0945]The magnifying lens 453 is attached to the eyepiece ring 452. An observer changes the insertion point within the body 451, and he adjusts the eyepiece ring 452 so that the display image of a display panel may be focused. If the positive lens 454 is arranged to the optical display panel's outgoing radiation side if needed, the chief ray which enters into the magnifying lens 453 can be completed. Therefore, the lens diameter of the magnifying lens 453 can be made small, and a viewfinder can be miniaturized.
[0946]Drawing 207 is a perspective view of a video camera. A video camera possesses the taking lens 461 and the video camera body 462, and the taking lens 461 and the viewfinder 466 are faced. The eyepiece covering 464 is attached to the viewfinder 466 (also see Drawing 206). An observer (user) observes the picture of a display panel from 464 copies of this eyepiece covering.
[0947]On the other hand, the EL display panel of this invention is used also as the display screen 21. The display screen 21 can adjust an angle freely with the fulcrum 468. It is stored in the storage 463 when not using the display screen 21.
[0948]In Drawing 207, 465 is a display mode changeover switch. If the display mode changeover switch 465 is pressed down, the circuit of drawing 44 will operate, and the matter explained by drawing 44 is carried out.
[0949]The EL display of this embodiment is applicable not only to a video camera but an electronic camera as shown in Drawing 208. The display panel 82 is used as a monitor attached to the main part 472 of a digital camera. The display mode changeover switch 465 besides the shutter 471 is attached to the main part 472 of a digital camera.
[0950]As for this display mode changeover switch 465, attaching to a cellular phone etc. is preferred. It is preferred to also add the function which changes the display luminance of the display mode changeover switch explained previously to a cellular phone etc. Hereafter, how to change this display luminance in digital one is explained.
[0951]Although drawing 80 etc. explained, N times as much current is sent through one of the drive methods of this invention at EL element 15, and there is a method of making only the period of 1/M of 1F turn on. By changing only the value of M of this 1/M made to turn on, a luminosity can be changed in digital one. For example, 4 times as much current is sent through EL element 15 as N= 4. If a lighting period is set to 1/M and it changes to M= 1, and 2, 3 and 4, the luminosity change from 1 time to 4 times will be attained. It may constitute so that it can change with M= 1, 1.5, 2, 3, 4, 5, 6, etc.
[0952]When one [the power supply of a cellular phone], after the above switching action displays the display screen 21 very brightly and passes fixed time, in order to carry out the electric power save of it, it uses for the composition in which display luminance is reduced. It can use also as a function set as the luminosity which a user wishes. For example, outdoors, it is bright in the circumference, and since a screen completely disappears, a screen is made very bright. However, if it continues expressing as high luminosity, EL element 15 will deteriorate rapidly. Therefore, when making it very bright, it constitutes so that it may be made to return to the usual luminosity for a short time. When making it display with high-intensity, and a user pushes a button, it constitutes so that display luminance can be made high.
[0953]therefore -- or a user is changed with a button, or it can change automatically in setting-out mode, or it detects the luminosity of outdoor daylight and it changes automatically -- a thing -- it is preferred to have composition [like]. It is preferred to constitute so that a user etc. can set display luminance to 50%, 60%, and 80%.
[0954]As for a display screen, it is preferred to use a Gaussian distribution display. A Gaussian distribution

display has the bright luminosity of a center section, and is a method which makes a periphery comparatively dark. If bright in a center section, a periphery will be sensed visual to be bright with it being dark. If the periphery is maintaining 70% of luminosity as compared with the center section according to subjectivity evaluation, it is visually equal. It is made to decrease furthermore and a problem does not have 50% mostly as luminosity. It is making down generate Gaussian distribution from on a screen in the self-luminescence type display panel of this invention using a pulse drive (how to send N times as much current through EL element 15, and to make only the period of 1/M of 1F turn on), N times explained previously.

[0955]By the upper part and the lower part of a screen, the value of M is enlarged and, specifically, the value of M is made small in the center section. This is realizable by modulating the working speed of the shift register of the gate driver 12 etc. The luminosity abnormal conditions of a screen on either side are generated by carrying out the multiplication of the data and picture image data of a table. When peripheral luminance (field angle 0.9) is made 50% by the above operation, as compared with the case of 100% luminosity, about 20% of low power consumption is possible. When peripheral luminance (field angle 0.9) is made 70%, as compared with the case of 100% luminosity, about 15% of low power consumption is possible.

[0956]As for a Gaussian distribution display, it is preferred to provide a changeover switch etc. so that it can turn on and off. For example, it is because a screen periphery will completely disappear outdoors etc. if it indicates by a gauss. therefore -- or a user is changed with a button, or it can change automatically in setting-out mode, or it detects the luminosity of outdoor daylight and it changes automatically -- a thing -- it is preferred to have composition [like]. It is preferred to constitute so that a user etc. can set peripheral luminance to 50%, 60%, and 80%.

[0957]Since fixed Gaussian distribution is generated with the back light in the liquid crystal display panel, Gaussian distribution cannot be turned on and off. An effect peculiar to a self-luminescence type display device can turn Gaussian distribution on and off.

[0958]When a frame rate is predetermined, it may interfere with the lighted condition of an indoor fluorescent lamp etc., and a flicker may occur.That is, if EL element 15 is operating by frame rate 60Hz when the fluorescent lamp is on by 60-Hz exchange, a delicate interference occurs and it may be sensed that the screen is blinking slowly. What is necessary is just to change a frame rate into avoiding this. This invention has added the change function of a frame rate. It constitutes so that the value of N or M can be changed in a pulse drive (how to send N times as much current through EL element 15, and to make only the period of 1/M of 1F turn on), N times.

[0959]The above matter is not limited only to a cellular phone and can be used for television, a monitor, etc. It is preferred to carry out an icon display to a display screen so that a user can recognize immediately in what kind of displaying condition it is shown. The above matter is the same also to the following matters.

[0960]It is preferred to carry the "screen automatic regulation" function to adjust a clock phase and a screen position (horizontal and vertical) automatically, and the "automatic gain control function" to adjust black level contrast automatically. If black level contrast is adjusted to a proper value, the optimal gradation display is realizable to each RGB color. It is preferred to carry the function to suppress the blot etc. which generate VGA mode etc. reduction or when an enlarged display is carried out. When not carrying out fixed time use, it is preferred to carry the "power save mode" in which a back light goes out automatically.

[0961]The value of M is considerably enlarged using a pulse drive (how to send N times as much current through EL element 15, and to make only the period of 1/M of 1F turn on), N times, and display luminance may be reduced to such an extent that a picture can be recognized slightly. Other this inventions of the above matter are the same.

[0962]The above is when the viewing area of the display panel 82 is comparatively small, but if it becomes large-sized with 30 inches or more, the display screen 21 will bend easily. For the measure, by this invention, as shown in Drawing 209, the outer frame 481 was attached to the display panel 82, and the holddown member 482 is attached so that the outer frame 481 may be hung and it may be lowered. As shown in Drawing 210 using this holddown member 482, it attaches to the wall 491 etc. using the holddown members 482, such as a screw.

[0963]However, weight will also become heavy if the screen size of the display panel 82 becomes large. Therefore, the leg mounting part 484 is arranged to the display panel 82 down side, and it enables it to hold the weight of the display panel 82 on two or more foot 483.

[0964]As shown in Drawing 209, the leg 483 is movable to right and left, as shown in A, and the leg 483 is constituted so that it can contract, as shown in B. Therefore, even if it is a narrow place, a display can be installed easily.

[0965]Plastic film metal plate composite (it is henceforth called composite) is used for the leg 483 or a case (also setting to other this inventions). Composite pastes up metal and a plastic film powerfully via a special-surface-treatment layer (glue line). 0.2 mm or more 0.8 mm or less of a metal plate is preferred, and, as for the plastic film stuck on a metal plate via a special-surface-treatment layer, it is preferred to use not less than 15 micrometers 100 micrometers or less. It comes to have firm adhesion power between a plastic and a metal plate with special adhesion method. By using this composite, the coloring to a plastic layer, dyeing, and printing are attained, and deletion of the fabricating process (****** of a film, plating paint) in a pressing is attained. In the former, it is suitable for impossible deep-drawing shaping or DI shaping.
[0966]The surface of a screen is covered with the protective film (a guard plate may be used) 493 in the television of Drawing 209. It is one purpose to prevent for an object to hit the display screen 21 of the display panel 82, and to damage this. It has controlled that an outer situation (outdoor daylight) is reflected to the liquid crystal display screen 21 by forming the AIR coat in the surface of the protective film 493, and carrying out embossing of the surface.
[0967]By sprinkling a bead etc. between the protective film 493 and the display panel 82, it constitutes so that fixed space may be arranged. Detailed heights are formed in the rear face of the protective film 493, and space is made to hold between the display panel 82 and the protective film 493 by these heights. Thus, the shock from the protective film 493 controls what is transmitted to the display panel 82 by holding space.
[0968]It is also effective to arrange or pour in optical coupling agents, such as solid resin, such as a fluid or gel acrylic resins, such as alcohol and ethylene glycol, or epoxy, between the protective film 493 and the display panel 82. While being able to prevent interface reflection, it is because said optical coupling agent functions as shock absorbing material.
[0969]As the protective film 493, a polycarbonate film (board), a polypropylene film (board), an acrylic film (board), polyester film (board), a PVA film (board), etc. are illustrated. In addition, engineering-plastics films (ABS etc.) can also be used. It may consist of inorganic materials, such as tempered glass. Instead of arranging the protective film 493, coating the surface of the display panel 82 with a thickness of 0.5 mm or more 2.0 mm or less with an epoxy resin, FENORU resin, and an acrylic resin also has the same effect. It is also effective in these resin surfaces to carry out embossing etc.
[0970]There is an effect also in carrying out the fluoride coat of the surface of the protective film 493 or coating material. It is because it can fail to wipe with a detergent etc. easily the dirt attached to the surface. A protective film may be formed thickly and may be used also [front light].
[0971]A screen may not be limited to 4:3 and a wide display display may be sufficient as it. As for resolution, it is preferred to use 1280x768 or more dots. By considering it as a wide type, the titles and programs of an oblong display, such as a DVD movie and television broadcasting, can be enjoyed by a full screen. the luminosity of the display panel 82 -- 300 cd/m^2 (a candela/square meter) -- further -- it is preferred to use 500 cd/m^2 (a candela/square meter). The changeover switch is installed so that it can display with a luminosity (200-cd[/m] ^{2}) suitable for the Internet or the usual personal computer work.
[0972]Thus, the user can make it the luminosity of the optimal screen with display information or directions for use. Only the window which furthermore shows the animation is made into 500 cd/m^2, and setting out made into 200-cd[/m] ^{2} is also possible for other portions. The TV program is displayed on the corner of the display and it can respond also to the usage of checking e-mail, flexibly. A speaker becomes the shape of a tower configuration, and it is designed so that a sound may spread not only to front but to the whole space.
[0973]Reproduction of a TV program and the recording function of user-friendliness are also improving. For example, reservation of picture recording from an I mode can be performed simply. Conventionally, after checking time and a channel in television program listings, such as a newspaper, it needed to reserve, but an electronic program guide can be checked and reserved by an I mode. Broadcasting hours are not known and troubled if it is this. Shortening reproduction of a picture recording program can also be performed. Judging importance by the existence of telops, such as a news program, or a sound, the portion judged to be unnecessary can be flown and the outline of a program can be seen in a short time (being a 30-minute program about 1 to 10 minutes).
[0974]Disk storage capacity is loading not less than 40 GB of hard disk so that television recording can be performed. This comprises an expansion box into which a power supply and the input/output terminal for images other than a main part were packed. Two visual equipment other than a personal computer and television is connectable with the expansion box used for connection of AV equipment, such as video. It

also has a switch terminal input besides D1 terminal for BS digital tuners, and the video input can choose it according to the apparatus to connect. The terminal for AV is arranged at the front face so that conveniently [connection of a game machine etc.].

[0975]The free installation united with the operating environment is attained by making a display screen into 30 procurvation or more and 120 retroflexion or more, and constituting so that it can rotate [270 degrees] in 90 degrees/180 degrees /. For example, it can be made to be able to rotate 90 degrees and a browser picture can be displayed longwise. A screen can be displayed toward the person who sat on the confrontation by carrying out retroflexion 145 degrees.

[0976]It cannot be overemphasized that the matter about the above protective film 493, a case, composition, the characteristic, a function, etc. is applied to other displays or information display devices of this invention.

[0977]Although one terminal of the capacitor 19 is connected with a Vdd power supply by drawing 61 etc., it is not limited to this. For example, one terminal may be connected to the gate signal line 17a of the preceding paragraph (pixel row before one) so that it may illustrate to Drawing 133. Although the gate signal line 17a of the preceding paragraph is chosen before 1H and potential fluctuation occurs, potential is fixed until it is chosen by the following 1F after that (until it is chosen next time). That is, since the gate signal line 17a1 of the preceding paragraph is being fixed to the OFF potential Vgh, it can be used as one electrode of the capacitor 19. Thus, the composition which uses the gate signal line of the preceding paragraph as an electrode of a capacitor is called preceding paragraph composition.

[0978]Although the gate signal line 17a is used as an electrode in Drawing 133, it may not be limited to this, and other gate signal lines may be used. The technical idea of preceding paragraph composition is a method which uses the fixed potential of the pixel which is not chosen. Therefore, latter gate potential can also be used depending on the case (for example, the gate signal line 17b, the reverse bias voltage Vm, etc.). It cannot be overemphasized that the above matter is applicable to other pixel configurations.

[0979]The same matter is applicable also to the pixel configuration of the voltage program of drawing 74. As preceding paragraph composition, the composition of Drawing 123 is illustrated and let one potential of the capacitor 19 be the potential of the gate signal line 17a1. The preceding paragraph composition of drawing 76 serves as Drawing 124. As mentioned above, by adopting preceding paragraph composition, the number of power supply wiring formed in a pixel can be decreased, and high numerical aperture-ization can also be realized.

[0980]Although already explained, TFT11d of drawing 61, TFT11e of drawing 62, TFT11d of drawing 63, TFT11b of drawing 64, TFT11d of drawing 65, TFT11d of drawing 66, By controlling on-off states, such as TFT11e of drawing 67, TFT11e of drawing 68, TFT11d of drawing 69, TFT11d of drawing 71, TFT11d of drawing 72, TFT11e of drawing 74, and TFT11e of drawing 75, It cannot be overemphasized that the drive method, the method of presentation, or the device explained with drawing 38, drawing 42, drawing 48, drawing 50, drawing 52 - drawing 54, drawing 57, drawing 59, drawing 60, Drawing 191, etc. can be carried out.

[0981]As for TFT11b for a drive, such as drawing 6, TFT11c for taking in, etc., being formed by N channel is preferred. the capacitor 19 -- it is because it runs and voltage decreases. Since off-leak of the capacitor 19 also decreases, it can apply also to a low frame rate of 10 Hz or less.

[0982]On the contrary, the method of poking by using TFT11b for a drive of drawing 6 and TFT11c for taking in as P channel, generating an omission, and indicating it good by black more is also effective. When TFT11b for a drive turns off in P channel, it becomes OFF state voltage Vgh. Therefore, the terminal voltage of the capacitor 19 shifts a few to the Vdd side, the gate terminal voltage of TFT11a for conversion rises, and it becomes a black display more. Since the current value considered as the 1st gradation display can be enlarged (base current fixed by the gradation 1 can be sent), the shortage of write current is mitigable with a current programming method.

[0983]In addition, the composition which forms and runs through a capacitor positively and makes voltage increase between the gate terminals of the gate signal line 17a and TFT11a for conversion is also effective (see Drawing 211). As for the capacity of this capacitor, it is preferred to use 1/10 or less [of the capacity of the capacitor 19 / 1/50 or more] and 1/15 or less [1/40 more or more]. Or the thing of the sauce gate (SG) of TFT11b for a drive or gate drain (GD) capacity further carried out to more than twice as many 6 or less times of SG (or GD) capacity as this 10 or less times 1 or more times is preferred. The formation position of a capacitor may be formed or arranged between one terminal (gate terminal of TFT11a for conversion) of the capacitor 19, and the source terminal of TFT11d for switching (see Drawing 212). It is the same as that of the value which explained capacity previously also in this case.

[0984]Therefore, TFT11b for a drive is used as P channel, and this P channel is made desirable on double-

gate ** at least more than a triple gate. Four or more gates are used still more preferably. And it is preferred to form or arrange the sauce gate (SG) of TFT11b for a drive or a capacitor with a [10 or less times of gate drain (GD) capacity (capacity when one / TFT /)] of of 1 or more times in parallel.
[0985]Not only the pixel configuration of drawing 6 but other pixel configurations of the above matter are effective. For example, in the pixel configuration of the current mirror of drawing 8 and drawing 9, the capacitor made to generate a thrust omission is arranged or formed between the gate terminals of the gate signal line 17a or 17b and TFT11a for conversion (see Drawing 213 and Drawing 214). N channel of TFT11c for taking in is carried out a double-gate ** top. Or TFT11c for taking in and TFT11d for switching are used as P channel, and it is made more than a triple gate. If it is in the composition of the voltage program of drawing 75, a capacitor is formed or arranged between the gate terminals of the gate signal line 17c and TFT11a for a drive. TFT11c for taking in uses more than a triple gate. The above matter is effective also in pixel configurations, such as Drawing 110 and drawing 76.
[0986]The capacitor 19b which runs and is made to generate voltage is formed with the source wiring and the gate wire of TFT. However, this expands the sauce width of TFT11, and since it is the gate signal line 17 and the composition formed in piles, there is a case of composition of that it is clearly inseparable with TFT practically. The method of running and constituting the capacitor 19b for voltage from forming greatly more than needed TFT11b for a drive and TFT11c for taking in (in the case of the composition of drawing 6) seemingly, is also a category of this invention. TFT11b for a drive and TFT11c for taking in are formed in many cases at channel width W / channel length L= 6 / 6 micrometers. Enlarging such channel width W also runs and the capacitor 19b for voltage can be constituted. For example, or more 2:1 the composition which makes the ratio of W:L preferably 10:1 or less [3:1 or more] 20:1 or less is illustrated in the ratio of W:L.
[0987]It runs and, as for the capacitor 19b for voltage, it is preferred to change a size (capacity) by R, G, and B which a pixel modulates. It is because the driving current of each EL element 15 of R, G, and B differs and the voltage (current) programmed to the gate terminal of TFT11a for conversion of EL element 15 differs. For example, when the capacitor 19b of R pixel is 0.02 pF, the capacitor 19b of other colors (pixel of G and B) shall be 0.025 pF. When the capacitor 19b of R pixel is 0.02 pF, it is that the capacitor 19b of G pixel shall be 0.03 pF, and the capacitor 19b of B pixel shall be 0.025 pF etc. Thus, the driving current of offset can be adjusted for every RGB by changing the capacity of the capacitor 19b for every pixel of R, G, and B. Therefore, the black display level of each RGB can be made into an optimum value.
[0988]It may run in the right and left of the display screen 21, and the capacity of the capacitor 19b for voltage may be changed. Since this has the gate driver 12 in the signal supply side, when the standup of a gating signal is quick (a slew rate is high), run, and voltage becomes large and gate signal line 17 end, It is because voltage becomes run and small, when the standup of a gating signal is late (a slew rate is late) since the signal wave form has become blunt. Therefore, the capacitor 19b by the side of connection with the gate driver 12 is made small, and the capacitor 19b of gate signal line 17 one end is enlarged. For example, the capacity of a capacitor is changed about 10% by the right and left of a screen.
[0989]As shown in Drawing 211 and Drawing 212, the composition which forms the capacitor 19b of this invention (arrangement) is as follows. That is, and it turns off after that. [TFT for switching] It is the composition of functioning in the direction keep the current of TFT11 from flowing into, by acting on the capacitor 19a etc. and changing the gate terminal of TFT11 (drawing 6 TFT11a) of EL element 15 for conversion at this time. Also in the case of N channel, although it was a case of P channel in Drawing 211 and Drawing 212, it is applicable so that it may illustrate to Drawing 215. In the case of N channel, and TFT turns it off on Vgl voltage. [Vgh voltage] [TFT] Therefore, what is necessary is in the case of N channel, just to constitute so that TFT11a for conversion may act in the direction which does not send current when TFT11b (11c) turns off from one (the pixel row is chosen) (the next pixel row is chosen). Therefore, when TFT to choose is come by off, this invention is constituted so that it may be made to operate in the direction which does not send current through EL element 15.
[0990]Since Drawing 215 is changed into P channel and N channel of TFT of drawing 6, and operation is the same as that of drawing 6, Drawing 211, etc., explanation is omitted. Since drawing 8 is also the same, this invention runs through change with P channel and N channel, and it can apply the concept of the capacitor 19b for voltage to other pixel configurations as it is.
[0991]The above matter can be made to apply also to the pixel configuration of voltage programs, such as drawing 75 and drawing 76. That is, it is because it can avoid sending current through EL element 15 if it does not become more than the program voltages more than fixed. Therefore, in a black display etc., when the signal is shaking in the noise, a noise level can be removed (it runs and a fixed level does not turn on EL element 15 by the effect of voltage).

[0992]Although it presupposed that it runs and voltage is set up by the capacity of the capacitor 19b (a desired value is used) in the above example, it runs and the value of voltage changes also the amplitude value of the gate signal line 17. Therefore, by adjusting the amplitude value of the gate signal line 17a (in the case of drawing 6), it runs and voltage can be adjusted. For example, amplitude value is 10V if it is Vgh voltage =10V of a gate signal line, and Vgl voltage =0V. Amplitude value will be set to 12V, if it runs in this state, it supposes that voltage is 0.1V and Vgh voltage is set to 12V. Therefore, it runs ideally and voltage is set to 0.12V. That is, it runs freely with the amplitude of the gate signal line 17, voltage can be changed, and base current can be adjusted now.
[0993]Since what is necessary is just to enable it to set up the value of Vgh voltage or Vgl voltage for the power supply circuit which generates gate voltage by a command, this control is easy. By adjusting this voltage, it runs and delicate adjustment of voltage is attained.
[0994]It will run, if the slew rate (change of potential to a standup and falling time) of the signal (on-off signal of TFT11) impressed to the gate signal line 17a is high, and voltage tends to increase. On the contrary, it will run, if a slew rate is low, and voltage falls. That is, the direction whose slew rate is 40v/microsec runs rather than 20v[/micro] sec, and voltage becomes large. The slew rate of this gating signal changes by the driving ability of the output buffers (an inverter circuit, an operational amplifier, etc.) of the gate driver 12. By controlling the output current of an output buffer, a slew rate can be adjusted, it runs and voltage can also be adjusted. the applied waveform to that controlling the output current of an output buffer adjusts the service voltage of an output buffer, and a gate terminal -- ****** -- it is realizable by things etc. It is easy on circuitry to adjust service voltage. the applied waveform to a gate terminal -- ****** -- by making size of the buffer of the preceding paragraph small (capability is reduced), things are realizable. It runs through the on-off signal impressed to the gate signal line 17a also as a sine curve or a serrate signal, and voltage can be changed. The above matter is applied also in control of the voltage control signal wire explained below and common signal lines.
[0995]In Drawing 211 etc., by running, although the capacitor 19b for voltage generating presupposed that one electrode is made into the gate signal line 17 (it was presupposed that it connects with the gate signal line 17), it is not limited to this. For example, it runs and the voltage control signal wire for control of the capacitor 19b is separately formed in voltage generating. The composition which connects one side to the gate terminal of TFT11a for conversion between two electrodes of the capacitor 19b, and is connected to said voltage control signal wire which formed another side separately may be used. It synchronizes with the selective state of the gate signal line 17a in this composition, and is a pulse signal (not limited to a square wave.) to a voltage control signal wire. a sine curve and a serrate signal -- it may be -- what is necessary is just to impress By adjusting this pulse amplitude value, it runs and voltage can be adjusted easily.
[0996]The signal wire insulated with said electrode may be formed in the lower layer of the electrode of the capacitor 19a. Temporarily, this signal wire is called common signal lines. If such composition is realized, the 2nd capacitor can be formed by common signal lines, said insulator layer, and the electrode of a capacitor. It can be considered that this capacitor is the capacitor 19b of Drawing 211. Therefore, the same operation and effect as the point can be demonstrated by impressing a PASURU signal to common signal lines like the point.
[0997]Common signal lines and a voltage control signal wire are formed in a pixel row and parallel. That is, said signal wire is formed for every pixel row (arrangement). However, it is not necessarily limited to forming for every pixel row. For example, what is necessary is just to form said signal wire for two or more pixel line of every, when choosing two or more pixel rows of pixels at a time (or arrangement).
[0998]In Drawing 211 etc., although 19b considered it as the capacitor of two terminals, it is not limited to this. For example, it is good also as a capacitor using the sauce inter gate capacity of TFT using TFT. That is, as long as the element which runs and generates voltage is not limited to a capacitor, is an insulating state and can change the potential of this terminal into the gate terminal of TFT11a for conversion of EL element 15, any may be sufficient as it. Of course, it cannot be overemphasized that a capacitor can be constituted also from a junction capacitance of a diode.
[0999]Although the capacitor 19b presupposed that it forms in each pixel, it is not necessarily limited to this. For example, the one capacitor 19b may be formed by the pixel which adjoined.
[1000]By arranging switching elements, such as TFT, at the end of the capacitor 19b (formation), and carrying out on-off control of this switching element, it may constitute so that the capacitor 19b can be separated from the pixel 16. That is, base current can be changed now by separating the capacitor 19b from the pixel 16 (it is and nothing). Although the capacitor 19b is separated by a switching element, control which sets capacity of the capacitor 19b to 0 may be performed by forming TFT (switching element) etc. which short-circuit inter-electrode [of the capacitor 19b] (arrangement), and making this

switching element one.
[1001]The object of change of potential is not limited to TFT11a for conversion. Any may be sufficient as long as it is an element which sets up the current amount of EL element 15. That is, it is because TFT11a for conversion can be constituted also from MIM and TFD (thin-film diode). What is necessary is just to constitute by controlling these, so that the current which flows into EL element 15 (or it passes) can be controlled. In this composition, a cathode terminal is processed into horizontal stripe shape if needed (formation).
[1002]It is a technical idea of this invention to control the current sent through EL element 15. Therefore, it runs and the generating timing of voltage is not conditions with the ability of the synchronization to not necessarily be taken [indispensable] with the scanning timing of the gate signal line 17a. Probably, nonsynchronous control will also be possible. It may run, and voltage may be distributed and impressed to multiple times.
[1003]As illustrated to Drawing 111 - Drawing 114, although current is outputted to the source signal line 18 in the current output circuit 1222 including the DA circuit 1226, In the case of the method of running, making generate voltage, as shown in Drawing 211, Drawing 212, and Drawing 215, and driving, it is necessary to add and output fixed base current. For example, when carrying out current programming of the current of 30nA to the pixel 16 with a certain gradation, the current which ran and added the base current by voltage is impressed to the source signal line 18. If base current is 40nA, the current of 30nA+40nA will be impressed to the source signal line 18 (it absorbs toward the current output circuit 1222 from the source signal line 18). Therefore, it is necessary to carry out circuitry so that base current may be added and sent. For example, the composition which adds the current mirror circuit for base current is illustrated.
[1004]Although it presupposed that current is outputted to the source signal line 18 in the current output circuit 1222 including the DA circuit 1226 in Drawing 111 - Drawing 114, it is not limited to this. For example, the 1st one current mirror circuit that generates reference current is formed in the source driver 14. It enables it to adjust the amount of output current of the whole source driver by adjusting the current sent through this 1st current mirror circuit. The luminosity of a display panel and the gamma characteristic can be adjusted with adjustment of this output current. Since a gamma curve differs from force current by RGB, reference current is constituted so that it can adjust uniquely for every R, G, and B pixel.
[1005]The method of constituting the 3rd 63 current mirror circuit (in the case of 64 gradation) of constituting two or more 2nd current mirror circuits that send the same current as this 1st current mirror circuit, and sending the same current as this 2nd current mirror circuit may be used. With data, the output current of this 3rd current mirror circuit is changed (the number to connect is changed), and it may enable it to impress predetermined current to the source signal line 18.
[1006]To the data D0 at one current mirror circuit and the data D1 In addition, two current mirror circuits, To the data D2 at four current mirror circuits and the data D3 Eight current mirror circuits, Correspond 16 current mirror circuits to the data D4, and 32 current mirror circuits are made to correspond to the data D5, the current mirror circuit connected corresponding to each data bit is made one, and the output of this total is impressed to the source signal line 18 -- it may constitute like (current is absorbed from a source signal line). A three-stage is used as mentioned above by clustering the 1st and 2nd current mirror circuits within 1 chip, and forming them in order to lessen variation in the output current outputted to the 3rd current mirror circuit and source signal line 18.
[1007]When it runs and the capacitor 19b for voltage is formed as shown in Drawing 211 and Drawing 215 even if it is the composition of the above-mentioned three-stage current mirror circuit, it is necessary to add and output fixed base current. For example, like the point, when carrying out current programming of the current of 30nA to the pixel 16 with a certain gradation, the current which ran and added the base current by voltage is impressed to the source signal line 18. If base current is 40nA, the current of 30nA+40nA will be impressed to the source signal line 18 (it absorbs toward the current output circuit 1222 from the source signal line 18). Therefore, it is necessary to carry out circuitry so that base current may be added and sent. For example, the composition which adds the current mirror circuit for base current separately is illustrated.
[1008]Since a gamma curve differs from force current every EL element 15 of RGB, it is preferred to constitute so that base current can also be uniquely adjusted for every RGB, and to constitute so that on-off control can be carried out. It is because it will be generated by the black float depending on a picture if base current is impressed (current may be absorbed from the source signal line 18). Therefore, it enables it to adjust the optimal by making base current turn on and off. It is preferred to enable it to also set up turning on and off of base current uniquely for every RGB.

[1009]Reference current and base current carry out temperature compensating. A panel (correctly temperature of EL element 15) is detected, and the value of reference current and base current is changed with the detected temperature. Generally, since luminous efficiency will fall if temperature goes up, EL element 15 is constituted so that the current impressed to EL element 15 may be increased, when temperature goes up. Also as for the temperature compensating of reference current and base current, it is preferred to enable it to set up a compensation value uniquely for every RGB.
[1010]In the above example, although EL element 15 presupposed that they are R, G, and B, it is not limited to this. For example, cyanogen, yellow, and magenta may be sufficient and two arbitrary colors may be sufficient. They may be six colors of R, G, B, cyanogen, yellow, and magenta, or four arbitrary colors or more. It may be white monochrome and what set white monochromatic light to RGB with the light filter may be used. It may be not the thing limited to an organic EL device but an inorganic EL element.
[1011]As for the gate driver 12 and the source driver 14, in the liquid crystal display panel of this invention, or the display using it, it is preferred that more than one (two or more kinds) are accumulated. By carrying out like this, pictures which enter from all communications networks, such as the animation and still picture which were downloaded from a portable telephone network or wireless LAN, and a picture which receives terrestrial television broadcasting, can be displayed, without applying a burden to MPU. High definition images are displayed using the 6-bit gate driver 12 and the source driver 14 by VGA correspondence, if a definition falls, they will be changed to QVGA, and if they are text data, they will use the 1-bit gate driver 12 and the source driver 14. It is also preferred to form the driver for an NTSC display (an interlace, false interlace scanning) and the driver for progressive displays (non-interlaced) separately. It cannot be overemphasized that the gate driver 12 and the source driver 14 which have two or more of these functions may be formed with a silicon chip, and it may mount by COG technology etc.
[1012]In drawing 34 and drawing 35, although the active-matrix type display panel was illustrated and explained, it is not limited to this. the N time current of predetermined current is impressed to the source signal line 18 from the source driver 14 etc. (from -- absorption). Two or more pixel rows are chosen simultaneously. And the concept that current is sent through an EL element and other periods do not send current can apply during a predetermined period also to a simple matrix type display panel.
[1013]When the number of the gate driver 12 and the source drivers 14 is one, in order to display the picture from which a definition differs, it is necessary to perform the conversion process of a signal by MPU. Since it is necessary to mount IC individually to prepare many gate drivers 12 and the source driver 14 except a liquid crystal display panel, a packaging area will be expanded while cost becomes high. Many circuits, such as the gate driver 12 and not only the source driver 14 but an image processing circuit, may be accumulated into the Si film on the display panel 82.
[1014]Since the characteristic change is large in early stages of lighting, an EL element is burned and tends to generate luck etc. After aging by a white raster display for less than 150 hours after panel formation for 20 hours or more for this measure, shipping as goods is preferred. It is preferred to make it display with an about 2 to 10-time luminosity rather than specified display luminosity in this aging.
[1015]Although the drive (display) method and the drive circuit were explained using drawing 10, drawing 38 - drawing 42, drawing 44, drawing 49, drawing 52, drawing 55, drawing 56, drawing 58, Drawing 137, Drawing 140 - Drawing 151, etc., The semiconductor chip produced in gallium arsenide, silicon, germanium, etc. which realize these technical ideas is also a scope of right of this invention. A display, an information display device, etc. are realizable by mounting these semiconductor chips in a display panel.
[1016]Good image display is realizable by connecting to the gate driver 12b the terminal which impresses the Vbb voltage in drawing 6 (b), drawing 9, drawing 65, drawing 68, drawing 69, drawing 71, etc., as drawing 56 explained.
[1017]The matter about the power supply voltage Vdd etc. which were explained with Drawing 153, Drawing 193, etc. is also applied to all the pixel configurations or the display panel, information display device, or drive method of this specification. Also about drawing 2 - drawing 5, drawing 12 - drawing 21, drawing 25 - drawing 27, Drawing 132, Drawing 137, Drawing 140 - Drawing 151, Drawing 192, Drawing 194 - Drawing 196, Drawing 201, Drawing 204, Drawing 206 - Drawing 209, etc., all the pixel configurations of this specification or driver arrangement, a display panel, It cannot be overemphasized that it is applied to an information display device or a drive method.
[1018]The drive method of this invention explained with drawing 34, drawing 35, drawing 73, drawing 77 - Drawing 109, and a drive circuit, A still more characteristic effect is demonstrated by combining the method or composition which impresses reverse bias voltage to EL element 15 explained with Drawing 131, Drawing 134, Drawing 137, Drawing 140 - Drawing 151, etc. It cannot be overemphasized that these are also applicable to the pixel configuration explained with drawing 6, drawing 8, drawing 74 - drawing 76,

Drawing 136 - Drawing 151, Drawing 211 - Drawing 215, etc. These composition does not take explanation to that drawing 37 - drawing 40, and drawing 42 -49, drawing 52 - drawing 54, drawing 57, drawing 59, drawing 60, drawing 74, etc. are also realizable, either. It cannot be overemphasized that it is also effective to combine with composition without three sides of drawing 12 - drawing 21. moreover -- using such art -- display panels, such as drawing 2 - drawing 5, drawing 12 - drawing 21, drawing 25 - drawing 27, Drawing 132, Drawing 137, Drawing 140 - Drawing 151, Drawing 192, Drawing 194 - Drawing 196, Drawing 201, Drawing 204, Drawing 206 - Drawing 209,. It cannot be overemphasized that it is also applicable to an information display device or a drive method.

[1019]The method or composition which impresses reverse bias voltage to EL element 15 explained with Drawing 131, Drawing 134, Drawing 137, Drawing 140 - Drawing 151, etc., It cannot be overemphasized that it applies to a pixel configuration or array constitution, such as drawing 6, drawing 8, drawing 38, drawing 51, drawing 55, drawing 56, drawing 61 - drawing 65, drawing 68 - drawing 72, drawing 74 - drawing 76, Drawing 123 - Drawing 130, Drawing 133, Drawing 137, Drawing 140 - Drawing 152, Drawing 211 - Drawing 215, etc. These composition does not take explanation to that drawing 37 - drawing 40, and drawing 42 - 49, drawing 52 - drawing 54, drawing 57, drawing 59, drawing 60, drawing 74, etc. are also realizable, either. It cannot be overemphasized that it is also effective to combine with three-side free composition, such as drawing 1, drawing 12 - drawing 21, Drawing 155 - Drawing 167, Drawing 173 - Drawing 176. In particular, in three-side free composition, it is effective when the pixel is produced using amorphous silicon art. It is preferred to carry out the current drive of this invention in the panel formed with amorphous silicon art, since the process control of characteristic dispersion of a TFT element is impossible.

[1020]furthermore -- using such art -- display panels, such as drawing 2 - drawing 5, drawing 12 - drawing 21, drawing 25 - drawing 27, Drawing 132, Drawing 137, Drawing 140 - Drawing 151, Drawing 192, Drawing 194 - Drawing 196, Drawing 201, Drawing 204, Drawing 206 - Drawing 209,. It cannot be overemphasized that it is also applicable to an information display device or a drive method.

[1021]The pixel configuration explained with Drawing 136 - Drawing 151, etc., the pixel configuration in a drive method, or array constitution is not limited only to an EL display panel. For example, it is applicable also to a liquid crystal display panel. What is necessary is just to transpose EL element 15 to light modulation layers, such as a liquid crystal layer, PLZT, and LED, in that case. It is not limited for a switching element to TFT. It cannot be overemphasized that it is applied to all the pixel configurations or driver arrangement, the display panel, information display device, or drive method of this specification.

[1022]Pixel configurations, such as drawing 6, drawing 8, drawing 17 - drawing 21, drawing 38, drawing 51, drawing 55, drawing 56, drawing 61 - drawing 65, drawing 68 - drawing 72, drawing 74 - drawing 76, Drawing 123 - Drawing 130, Drawing 133, Drawing 137, Drawing 140 - Drawing 152, Drawing 211 - Drawing 215. Or array constitution is not limited only to an EL display panel. For example, it is applicable also to a liquid crystal display panel. What is necessary is just to transpose EL element 15 to light modulation layers, such as a liquid crystal layer, PLZT, and LED, in that case. Drawing 193 etc. explained that it was not what is limited also for a switching element to TFT.

[1023]The composition of drawing 3, drawing 12, drawing 15, drawing 17 - drawing 21, Drawing 132, Drawing 199, Drawing 201, Drawing 202, Drawing 206 - Drawing 209, etc., a device, and a method are not limited to what used the EL display panel. For example, it is applicable also to the thing using a PDP display panel, a PLZT display panel, a liquid crystal display panel, etc.

[1024]A pixel configuration or array constitution, such as drawing 6, drawing 8, drawing 28, drawing 38, drawing 51, drawing 55, drawing 56, and drawing 61 -65, drawing 68 - drawing 72, drawing 74 - drawing 76, Drawing 123 - Drawing 130, Drawing 133, Drawing 137, Drawing 140 - Drawing 152, Drawing 211 - Drawing 215, It cannot be overemphasized that it is applicable to information display devices, such as Drawing 197, Drawing 198, Drawing 200, and Drawing 205.

[1025]A pixel configuration or array constitution, such as drawing 6, drawing 8, drawing 38, drawing 51, drawing 55, drawing 56, and drawing 61 -65, drawing 68 - drawing 72, drawing 74 - drawing 76, Drawing 123 - Drawing 130, Drawing 133, Drawing 137, Drawing 140 - Drawing 152, Drawing 211 - Drawing 215, It cannot be overemphasized that it is employable as drawing 3, drawing 12, drawing 15, drawing 17 - drawing 21, Drawing 132, Drawing 177 - Drawing 190, Drawing 197 - Drawing 202, Drawing 205 - Drawing 209.

[1026]If it is in the method of drawing 32 and drawing 33, it is not limited to the manufacturing method of an EL display panel. For example, it is applicable also to the manufacturing method of a liquid crystal display panel. It cannot be overemphasized that it is not limited to an EL display panel even if it is in the composition or the method of drawing 12 - drawing 21, and it can apply to a LED display panel, a liquid crystal display panel, etc. The same may be said of the methods of presentation, such as drawing 37 - drawing 40, drawing 42 - drawing 49, drawing 52 - drawing 54, drawing 57, drawing 59, drawing 60, and

drawing 74.
[1027]As mentioned above, the technical idea explained in the example of this invention is applicable to a video camera, a projector, stereoscopic television, projection TV, etc. It is applicable also to a viewfinder, the monitor of a cellular phone, PHS, a Personal Digital Assistant and its monitor, a digital camera, and its monitor. It is applicable also to an electrophotography system, a head mount display, an accepting-reality monitor display, a note personal computer, a video camera, and an electronic "still" camera. It is applicable also to the monitor of a cash automatic drawer machine, a public telephone, a TV phone, a personal computer, a wrist watch, and its display. It cannot be overemphasized to a display monitor, a pocket game machine machine and its monitor, a back light for display panels, or a for home use or business-use lighting system of homeuse-electronics apparatus, etc. that application or application deployment can be carried out. As for a lighting system, constituting so that a color temperature may be changed is preferred. This forms the pixel of RGB stripe shape or in the shape of a dot matrix, and can change a color temperature by adjusting the current sent through these. It is applicable to displays, such as an advertisement or a poster, the ringer of RGB, warning display light, etc.
[1028]The organic EL panel is effective also as a light source of a scanner. A subject is irradiated by using the dot matrix of RGB as a light source, and a picture is read. Of course, it cannot be overemphasized that monochrome may be sufficient. Not the thing limited to an active matrix but a simple matrix may be sufficient. If it enables it to adjust a color temperature, image reading accuracy will also improve.
[1029]The organic electroluminescence display is effective also in the back light of a liquid crystal display. The pixel of RGB of an EL display (back light) is formed stripe shape or in the shape of a dot matrix, and a color temperature can be changed by adjusting the current sent through these, and adjustment of a luminosity is also easy. Moreover, since it is the surface light source, the Gaussian distribution which makes a periphery dark for the center section of the screen brightly can be constituted easily. It is effective also as a back light of the liquid crystal display panel of a field sequential system which scans R, G, and B light by turns. Even if it blinks a back light, it can use also as a back light of the liquid crystal display panel for animation display by carrying out black insertion.
[1030]
[Effect of the Invention]The display panel of this invention, a display, etc. demonstrate a characteristic effect according to each composition of high-definition and good animation display performance, low power consumption, low-cost-izing, a rise in luminosity, etc.
[1031]Since the information display device of low power consumption, etc. can be constituted if this invention is used, electric power is not consumed. Since a small weight saving can be carried out, resources are not consumed. Even if it is a high definition display panel, it can fully respond. Therefore, he will be kind to earth environment and the space environment.

[Translation done.]